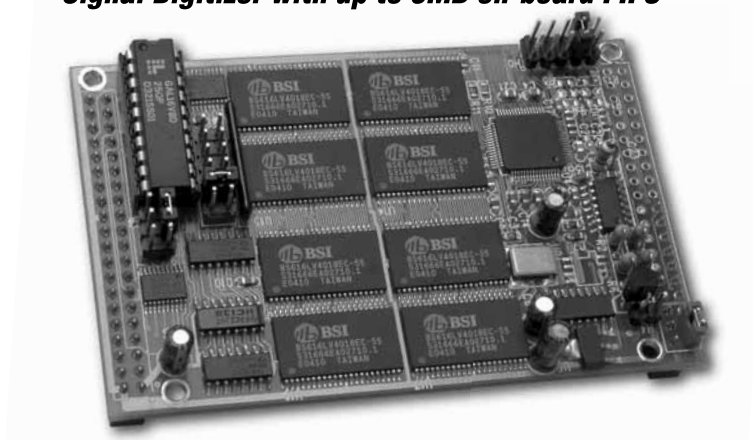
GR16™ *10M Samples Per Second, 16-bit ADC, 8MB FIFO*

NEW!

Single Channel High Speed (up to 10M SPS) Analog Signal Digitizer with up to 8MB on-board FIFO



Features:

- 2.3 x 3.6 x 0.5 inches
- 200 mA at 5V DC power
- High-Speed Delta-Sigma ADC (ADS1610)
- User Programmable Sample Rate, up to 10M SPS
- On-Chip Digital Filter Simplifies Anti-Alias
- User configurable FIFO data size, up to 8MB.
- Stackable multi units sharing Sync, and Trigger.
- On-board oscillator or external host clock.
- Driven be 16-bit TERN controllers
- Support ADC read, ADC-FIFO, FIFO-read modes

The **GR16™** is an inexpensive high speed (up to 10M samples per second), 16-bit analog signal digitizer, designed to be driven by a host TERN 16-bit controller, such as 586-Engine, AE86, or EE.

The **GR16™** supports a 16-bit Delta-Sigma ADC(ADS1610). With its outstanding high-speed performance, it is well-suited for demanding applications in data acquisition, scientific instruments, test equipment and communications.

ADC Sampling

Three operation modes are available: **ADC-read, ADC-FIFO,** and **FIFO-read**. In **ADC-read** mode, an application running on the host can read the 16-bit ADC data at any time. Sampling rate would be limited to CPU and application processing speed.

In **ADC-FIFO** mode, the board can sample at far faster speeds (up to 10M samples per second). This data is recorded into the on-board FIFO SRAM. The ADC-FIFO operation is done entirely in hardware, without using any host CPU time. Finally, the system can be set to **FIFO-read** mode. The host CPU can then read as much FIFO data as desired via I/O or DMA access.

The ADC sampling clock can be driven by on-board clock oscillator, or an external clock. With a 60MHz on-board oscillator, the sample rate is 10MHz maximum. User can control the sampling rate by using variable external clock, or selecting different dividers using onboard jumpers. The recording length of 16-bit ADC data can be configured via a jumper block. The available data length includes 8MB, 4MB or 512KB.

The **ADC-FIFO** operation starts on one software instruction (set AST low) and stops automatically as soon as the selected recording length reached. The FIFO will retain this data until power-off, or a new **ADC-FIFO** operation is initiated. The host controller can read any length of the FIFO but always starts at address zero.

Two analog inputs INP and INN are differential signals direct routed to the chip, without buffer circuits. External user circuits driving the ADS1610 inputs must be able to handle the load presented by the switching capacitors within the chip. Recommended circuit designs are available when using single-ended or differential op amps, respectively.

The 16-bit ADC data is in binary two's complement. With the on-board (VREFP – VREFN)=VREF=3V, if INP>INN, outputs 0-0x7FFF, and if INP<INN, outputs 0x8000-0xFFFF.

If INP-INN=3V, it outputs 0x7FFF. If INN-INP=3V, it outputs 0x8000. If INN=INP, it outputs 0 or 0xFFFF.

To achieve the highest analog performance, the recommended differential analog input voltage range is 3Vx0.891=2.67V. The absolute input voltage with respect to GND, on either INN or INP pin, must be within VREFN=1V to VREFP=4V range.

Multiple **GR16™** units can be stacked sharing common CLK and SYNC signals. With the CLK inputs running, pulse SYNC, multiple converters will convert synchronously simultaneously.

GR16 installed on top of AE86-P

The ADS1610 is a high-speed, 16-bit ADC designed for dynamic differential analog inputs other than precision still DC measurement. High speed sampling tends to be noisier. Special care must be taken when selecting the test equipment and setup used with this device.

The **GR16™** is designed as an expansion board, measuring 2.3 by 3.6 inches, for TERN 16-bit controllers such as A-Engine86, 586-Drive, EE, and FN. The GR16™ interfaces to Tern host controller via 20x2 pins at J1, and 10x2 pins at J2.

Ordering Information

GR16 $149 Qty 1

Includes: ADS1610, 512KB 55ns FIFO RAM.

NOT including add-on options. OEM option discounts available.

Add-on Options:

1) 55 ns 512KB x 8 SRAM (up to 5 MHz) $80
2) 45 ns 1MB x 8 SRAM (upto 10 MHz) $160

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