5E, 5D, or 5P supports MMC, P52, P100, UR8: *February 22, 2007*

586E, 5D, 5P can interface to MMC, P52, P100, UR8….via J1+J2
SC520 supports 8 GP-bus Chip selects, I/O mapping conflict occur and modifications/configurations are required.
Table below maps usage of 8 GP chip selects:

Chip Select	586E	586P	586D	P100	P51	P52	MMC	UR8
/CS0= 0x1800	P27=J2.37 16-bit AD/DA	P27=J2.37 FREE	P27=J2.37 FREE		i2Chip H7.1= H7.2	i2Chip H7.1= H7.2	/CSM H1.4=H1.6	
/CS1= ROM1 0x1000	J1.19 PAL,SCC ADC DAC 0x1000-7f	J1.19	U16 ROM socket	J1.19 uses 0x1080 To 0x10ff	AD,DA, PPI, /ADR PAL= P51P586	AD,DA, PPI, /ADR PAL= P52P000	/CSI=J1.19 H1.3=H1.5 /ADR 0x1000-7f AD/CF 0x1080-ff	J1.19 H7.3= H7.5 0x108 0-ff
/CS2= /ROM2	SRAM	SRAM	SRAM					
/CS3= PITG2= J4.1 0x2000	Add Wire J4.1=J2.23	J4.1 ADC CF	AD, SC1, SC2 CF, HV		H7.2= H7.3	i2Chip H7.2= H7.3 J2.23	/CSM H1.4=H1.2 /CSM= J2.23	
/CS4= TIN1= 0x2800	J4.6 FREE	J4.6 FREE	J2.1 FREE					
/CS5= TIN0= 0x3000	J4.4 FREE	J4.4 FREE	J1.19 FREE				/CSI=J1.19 H1.3=H1.5 /ADR 0x1000-7f AD/CF 0x1080-ff	
/CS6= TO1= 0x3800	J4.5 FREE	J4.5 FREE	J2.5 FREE					
/CS7= TO0=J4.3 0x4000	Add Wire J4.3=J2.22	Add Wire J4.3=J2.22	i2Chip J2.8		PAL= P51P586A		/CSI, H1.3=H1.1 /CSI=J2.22	

Example configuration:
5E+P100+MMC: On 5E, wires J4.1=J2.23 and J4.3=J2.22. On MMC, H1.2=H1.4 and wire H1.3=J2.22
5E+P51: On 5E, wires J4.1=J2.23 and J4.3=J2.22. P51 PAL=P51P586A
5E+UR8+P51: On 5E, wires J4.1=J2.23 and J4.3=J2.22. On P51, PAL=P51P586A. On UR8, H7.3=H7.5
5P+MMC: On MMC, H1.4=H1.6 and H1.3=H1.5.
5P+P51: On P51, H7.1=H7.2, PAL=P51P586.
5P+P100+MMC: On MMC, H1.4=H1.6 and H1.3=H1.5, must No ADC, No CF(conflict with P100).
5P+UR8+P51: On 5P, wires J4.3=J2.22. On P51, H7.1=H7.2, PAL=P51P586A. On UR8, H7.3=H7.5.
5P+UR8+P100x2QD:. On P100, PAL P100P000& P100P010. On UR8, H7.1=H7.3.