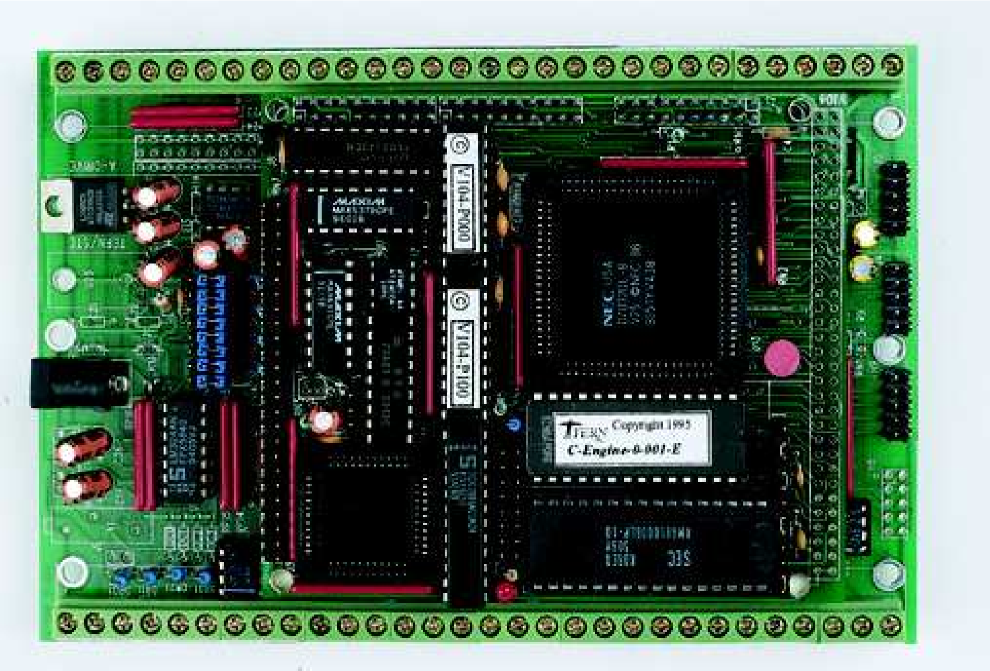
A-Drive™

Analog controller with 22 ADC inputs + 8 DAC outputs
Driven by the V104™



Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1 Introduction

1.1 Functional Description

The A-Drive is designed for industrial process control, automatic test equipment, and data acquisition applications that require many channels of analog signal I/Os.

The A-Drive features 22 channels of 12-bit ADC inputs and 8 channels of 12-bit DAC outputs. There are 6 instrumentation operational amplifiers providing high input impedance, high gain, low noise to low-voltage output sensors, such as EKG electrodes, thermocouples, or strain gauges. A precision temperature sensor (10 mV/C°) is located to the screw terminals for thermocouple cold junction compensation. A precision 3 ppm/C°, 2.5V reference supports 12-bit ADCs and DACs.

The 12-bit ADC features sample-and-hold and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range up to approximate 2500 Hz sample rate.

The 8 channels of 12-bit DAC can output either voltage or current via ops, default 0-2.5V or 4-20 mA. The DACs features power-on reset, 3µs output setting time and 5 V/µs slew rate. User may customize analog input and output ranges by setting different gain resistors.

There are 7 channels of solenoid drivers that can sink/source up to 500 mA at 50V. There are 2 16-bit counters and 3 external interrupt inputs. Schmitt-trigger inverters are provided for high-speed counter and interrupt inputs to increase noise immunity and transform slowly-changing input signals to fast-changing and jitter-free signals. There are two RS-232 serial ports and one RS-485 serial port.

The A-Drive must be driven by a V104. It features a 16-bit 8 MHz V25 CPU, three 16-bit timers, 3 serial ports, additional 24 bi-directional I/O lines of a 82C55, up to 512K battery backed-up SRAM, up to 512K EPROM or Flash EEPROM, 512 bytes of EEPROM, a LCD interface, a real time clock, a 64-pin PC/104 bus, a LED, and a supervisor chip providing power failure detection, watchdog timer, and reset.

All analog input and output signals are connected via screw terminals.

Features

- Measures 6.2 x 4.2 inches.
- Power consumption: 170 mA.
- Low power version: 85 mA full speed, 25 mA standby.
- *22* channels of 12-bit ADC, 2500Hz sample rate.
- Six channels of high gain (1000) instrumentation ops.
- Directly interface to thermocouples, RTD, or strain gauges.
- *8* channels of 12-bit DAC output 0-2.5 V or 4-20 mA.
- Two RS-232 channels and one networking RS-485 channel.
- On-board temperature sensor for cold-junction compensation.
- 2.5V, 3 ppm/C° precision reference voltage.
- Analog signal conditioning circuit for ADC and DAC.
- User configurable gain, filter, and offset.
- 16-bit CPU (NEC V25), 8 MHz.
- Up to 1MB Flash/EPROM and battery-backed SRAM.
- *24* bi-directional I/O lines free to use.
- *7* comparators inputs or *7* high voltage drivers.
- **3** 16-bit timers. **2** external event counter up to 500K Hz.
- Real-time clock RTC72421, coin battery, 512 byte EEPROM.
- Supervisor chip (691) for power failure, reset and watchdog.
- LCD interface and 64 pin PC/104 bus interface.
- **3** external interrupt inputs with Schmitt trigger buffers.
- On-board power supply for +5V, +7V, -12V, -5V and 2.5V.

How do you program the A-Drive™?

Development of application software for the A-Drive+V104 consists of three easy steps, as shown in the block diagram below.

STEP 1 Serial link PC and A-Drive, program in C/C++.
Debug and run application with remote Debugger.

↕

STEP 2 Test A-Drive in the field, away from PC.
Application program resides in the battery-backed SRAM.

↓

STEP 3 Burn application ROM.
Replace Debug ROM, project is complete.

You can program the A-Drive+V104 from your PC via serial link with an RS232 interface. Your C/C++ program can be remotely debugged over the serial link at a rate of 115,000 baud. The C/C++ Evaluation Kit (EV) or Development Kit (DV) from TERN provides a Borland C/C++ compiler, TASM, LOC31, Turbo Remote Debugger, I/O driver libraries, sample programs, and batch files. These kits also include a DEBUG ROM (*TDREM_V25)* to communicate with Turbo Debugger, a DB9-IDE10 (PC-V25) serial cable to connect the controller to the PC, and a 9-volt wall transformer. *See your Evaluation/Development Kit Technical Manual for more information on these kits.* Also, please see the V104 Technical Manual for more details.

Minimum Hardware and Software Requirements

Minimum Hardware Requirements:

- PC or PC-compatible computer with serial COMx port that supports 115,200 baud
- A-Drive + V104 controller with DEBUG ROM *TDREM_V25*
- DB9-IDE10 (PC-V25) serial cable (RS232; DB9 connector for PC COM port and IDC 2x5 connector for controller)
- center negative wall transformer (+9V 500 mA)

Minimum Software Requirements:

- TERN EV/DV Kit installation diskettes
- PC software environment: DOS, Windows 3.1, Windows95, or Windows98

The C/C++ Evaluation Kit (EV) and C/C++ Development Kit (DV) are available from TERN. The EV Kit is a limited-functionality version of the DV Kit. With the EV Kit, you can program and debug the A-Drive+V104 in Step One and Step Two, but you cannot run Step Three. In order to generate an application ROM/Flash file, make production version ROMs, and complete the project, you will need the Development Kit (DV).

A functional block diagram of the A-Drive+V104™ system is shown in Fig. 1.1.
Please see the V104 Technical Manual for more details.

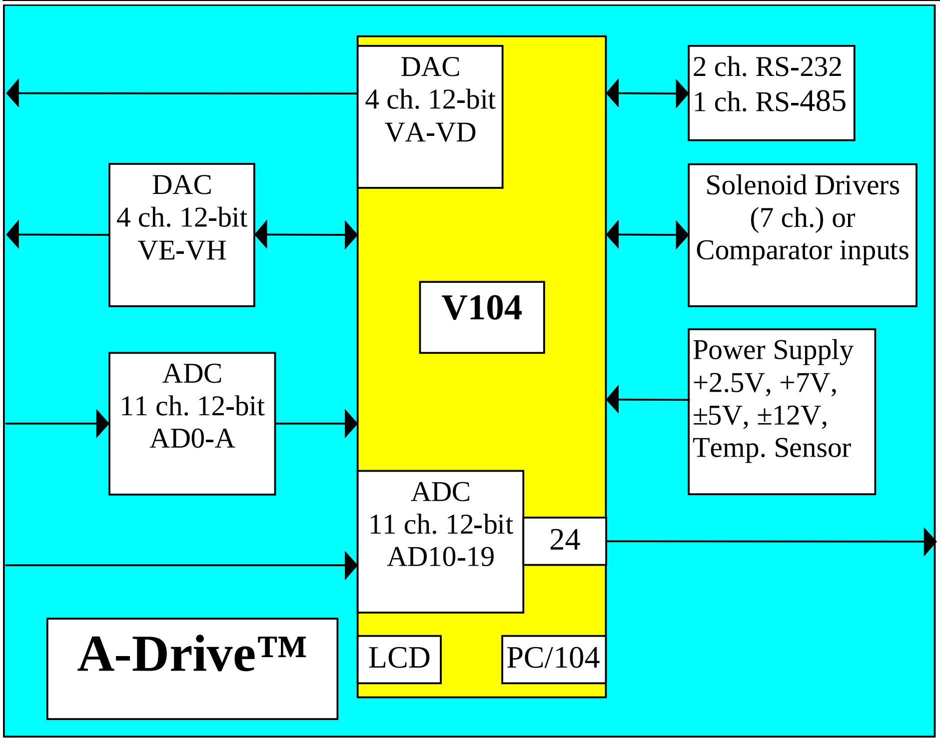


Fig. 1.1. Functional block diagram of the A-Drive+V104™ system

Physical Layout

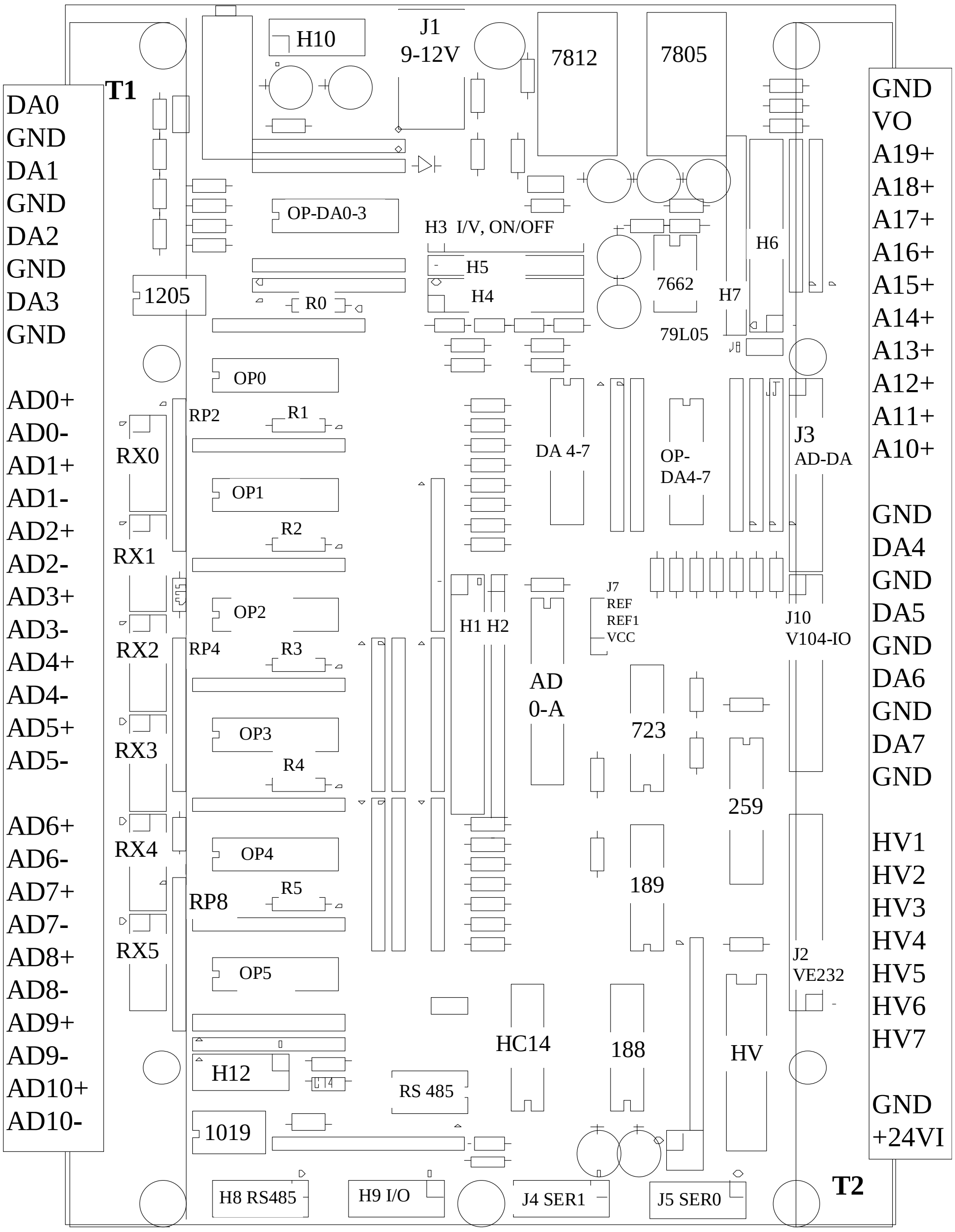


Fig. 1.2 Physical layout of the A-Drive™ without the V104™.

Components used in the A-Drive™ are listed below.

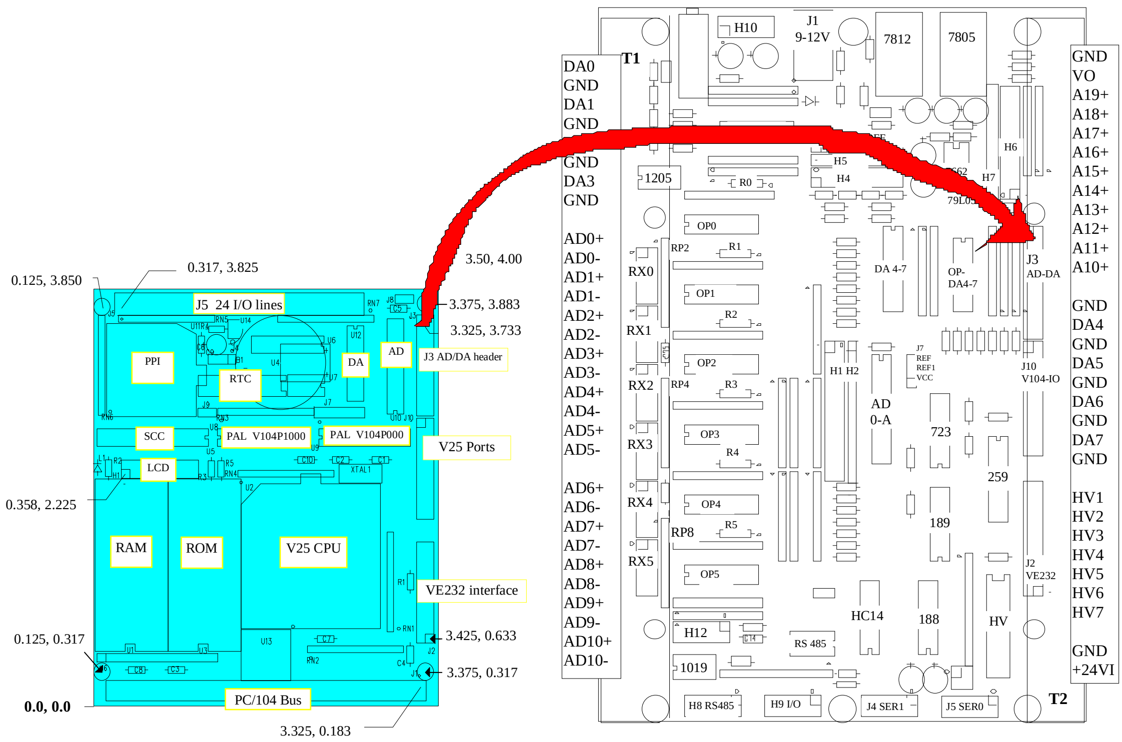
Item	Quantity	Reference	Part
1	24	C1,DC1,C2,DC2,C3,DC3,C4, DC4,C5,DC5,C6,DC6,C7,DC7 C8,C9,C10,C11,C12,C13,C14,C15,C0,DC0	100P
2	9	C16,C18,C20,C26,C27,C30,C31,C32,C33	DIPCAP
3	6	C17,C23,C24,C25,C28,C29	10UF35V

4	1	C19	100PF
5	2	C21,C22	0.01UF
6	1	D1	1N5817
7	21	DR01,R01,RP2,RP4,RP8,DR11,R11,DR21,R21,DR31 R31,DR41,R41,DR51,R51,DR61,R61,DR71,R71,R81,R91	100K
8	1	H1	HDRD12
9	5	H2,H3,H4,H5,H13	HDRD8
10	4	J2,J3,H6,J10	HDRD20
11	1	H7	HDRS10
12	11	RX1,RX2,RX3,J4,RX4,J5, RX5,H8,H9,H10,RX0	HDRD10
13	1	H11	HDRS6
14	3	H12,H14,H15	HDRS4
15	10	IV1,IV2,IV3,IV4,IV5,IV6, IV7,IV8,IV9,IV0	HDRD6
16	1	J1	DJ-005
17	3	J6,J8,J9	HDRD2
18	2	J7,J12	HDRS3
19	1	J11	HDRD4
20	6	R1,R2,R3,R4,R5,R0	1K
21	21	RP1,RP3,RP5,R6,RP6,RP7,RP9,RP10,RP11,RP12,RP13 RP14,RP15,R16,RP16,RP17,RP18,RP19,RP20,RP21,R22	10K
22	1	R7	3.3
23	2	R8,R10	680
24	1	R9	220
25	2	R12,R13	300K
26	1	R14	10.7K
27	1	R15	2K
28	2	RN1,RN2	RN10S1
29	4	RP22,RP23,RP24,RP25	RP8S1
30	2	T1,T2	T30
31	9	U0, U1,U2,U3,U4,U5,U6,U7,U8,	LM324A
32	1	U9	LT1025
33	1	U10	75C188
34	1	U11	74HC259
35	1	U12	LTC2543
36	1	U13	MAX537
37	1	U14	ULN2003/UDS2982
38	1	U15	LM79L05
39	1	U16	ICL7662
40	1	U17	LM723
41	2	U18,U21	TK112XX
42	1	U19	74HC14
43	1	U20	LM340
44	1	U22	LT1019
45	1	U23	LTC485
46	1	U24	1489
47	1	U25	LM7812
48	1	V1	POT

Chapter 2
Installation

2.1 Software Installation
See V104™ manual for software installation.

2.2 Hardware Installation
1. Install V104™ on the A-Drive™ via J2(10x2), J3 and J10(20x2) headers.



2. Connect the IDC10 connector of the PC-V25 serial cable to J5 of the A-Drive™, with the red side of the cable corresponding to pin 1 of J5 (a small circle close to J5 indicates pin number 1), and connect DB9 connector of the serial cable to COM1 or COM2, the PC serial port.

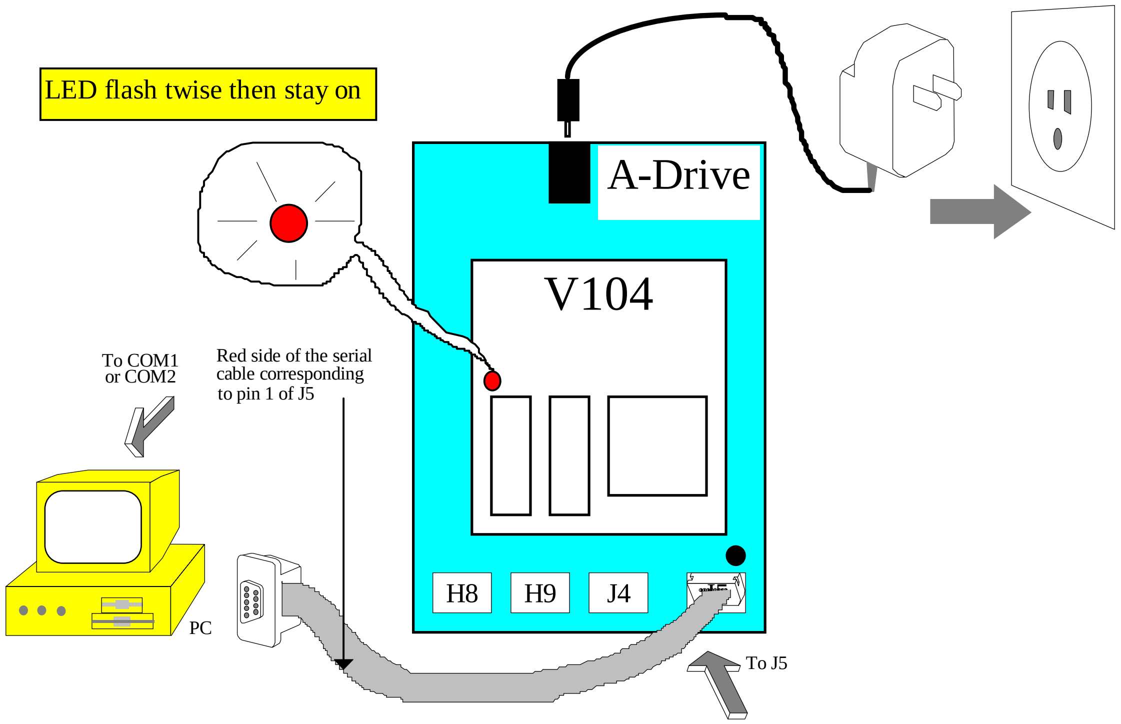


Fig. 2.1. Connect the MotionC™ to your PC COM1/2 via a PC-V25 serial cable.

Connect a center negative wall transformer (+9V DC) to the A-Drive™ DC power jack J1.

3. Simple Test

After the DC power on, the LED on the V104™ should flash twice and then stay on. You can run a simple sample program "**led.c**" under your default directory to test the software and hardware installation. The LED on the V104™ should blink while runing the led.c. The procedure involved in the test is described in the V104™ Manual.

Chapter 3
Hardware

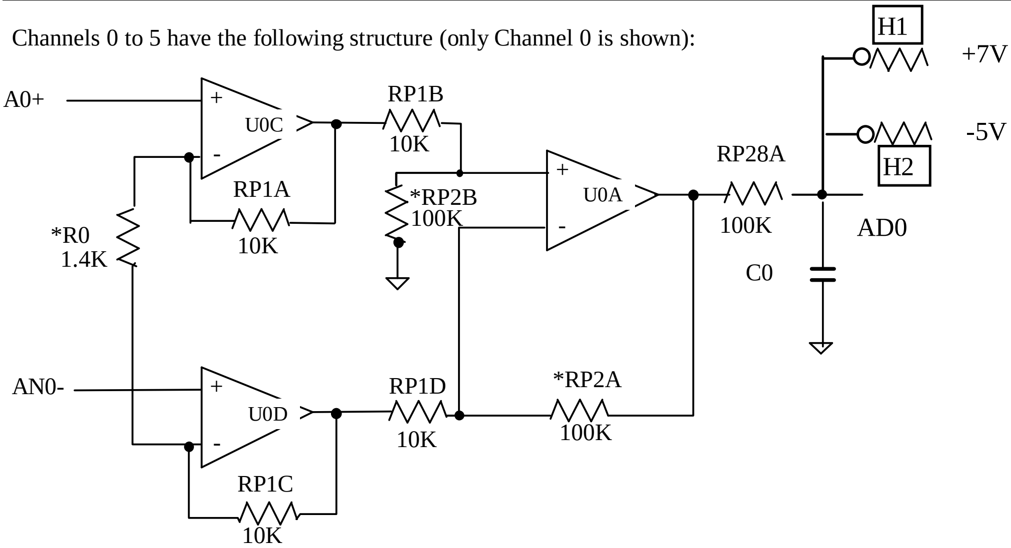
3.1 V104™
The A-Drive™ is driven by a V104™ module. Please refer to the V104™ Technical Manual for more information.

3.2 Interface with the V104™
The A-Drive™ interfaces with the V104™ via three 10x2 headers: J3, J10 and J2.
Please see A-Drive™ schematics for detail signal names.

3.3 Instrumentation Operational Amplifiers and analog signal conditioning

The analog signal conditioning circuit provides 6 channels of instrumentation operational amplifiers with high gain (>1000) and high input impedance ($>10^{12}\ \Omega$). The instrumentation ops allow direct interfacing to low-voltage output sensors, such as EKG electrodes, thermocouples, or strain gauges.
The high input impedance adjustable-gain differential amplifier is constructed with three operational amplifiers, see Fig 3.1.
Two operational amplifiers, UxD and UxC, are operated in the noninverting mode. The input impedance at each input pin of the differential amplifier is the common-mode input impedance of the Op chips, depending on the type of Ops used. For example, the input impedance of LM324 is typical 2M, LT1014 is typical 300M. The UxD and UxC constitute a differential buffer amplifier with a gain of G=1+2*RP1A/R0 (see schematics channel 0) for differential signals. The gain can be varied by a single resistor, R0. If RP1A=RP1C=10K, R0=1.40K, then approximately gain of the first stage G=15 , as factory setting. The effects of mismatch in RP1A and RP1C is only created a gain error without affecting the Common-Mode Rejection Ratio(CMRR). The CMRR, in term of the ratio of differential signal gain to common-mode signal gain, is typical 70db for LM324 and is typical 110db for LT1014. The third OP, U0A, is a differential-input to single-input converter. The offset voltages and the offset drifts of U0D and U0C are significant in determining the output offset. Since the output voltage drift is proportional to the differences of the voltage offsets of U0D and U0C, it is desirable to use low temperature drift OPs. For LM324 the maximum input offset voltage drift is 30 uV per degree C and the typical offset drift is 7 uV per degree C. For LT1014, the maximum offset drift is 2.5 uV/C. The typical input offset drift is 0.4 uV/C°.
The RP2 is 100K and RP1 is 10K. The second stage gain is default of 10. The total gain of the instrumentation op is approximately 150.
Type J thermocouples have a thermoelectric voltage change of 4.906 mV at 93 degree C(reference to 0 C). It is about 0.0528 mV/C°. For a 12-bit ADC with 2.5V reference, the resolution is 1.2207mV/LSB. For a gain of 150, the sensitivity can be approximately 6 LSBs per degree C.
The gain is configurable by changing the resistors with "*".
For the channel 6 to 10, single differential op-amp is used to condition the analog input signal. The default gain of these channels is set to 0.5, but configurable by changing the resistors with "*".
You may install an ***offset*** resistor in H1 or H2 to offset the Op output voltage to match the 0-2.5V valid ADC input voltage range.

Channels 0 to 5 have the following structure (only Channel 0 is shown):



The gain of the first stage: 1+2*RP1A/R0

The gain of the second stage: RP2A/RP1D

Channels 6, 7, 8, 9 and 10 have the following structure (only Channel 6 is shown): G=100K/200K=0.5

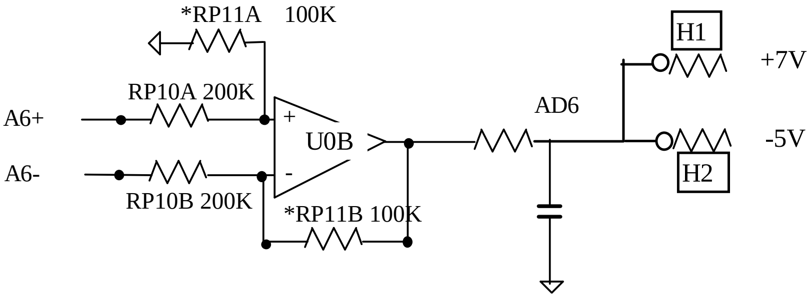
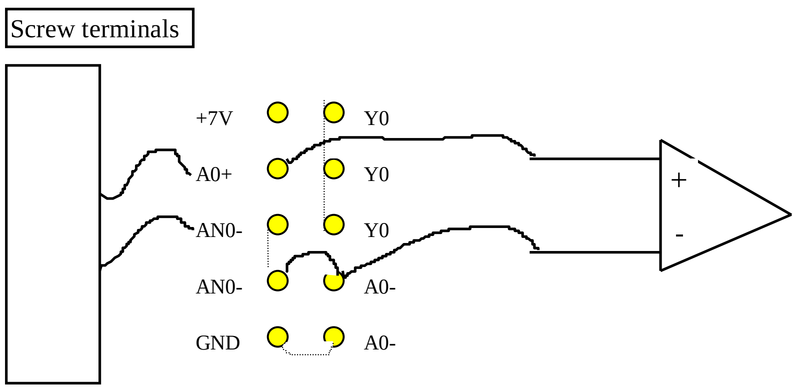


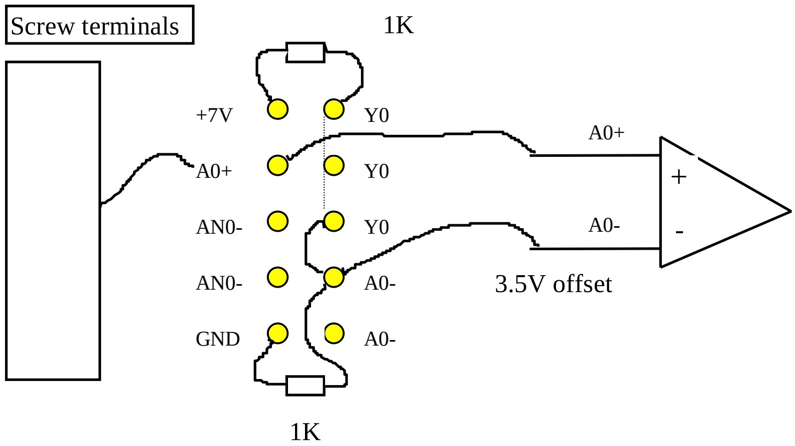
Fig 3.1, Analog signal conditioning

3.4 Front End Prototyping Pads

Rx0 to Rx5 are a total of six pads area designed for application prototype. You may install bridge resistors in that area. You also may set offset resistors or divider resistors in the prototyping aera. The default setting is AN0- wired to A0-, and A0- jumper to GND.



You may install offset resistors to set an offset voltage at A0-.



3.5 ADC

There are two ADC(TLC2543) chips: U10 V104-ADC and U12 A-Drive-ADC. The TLC2543 is a 12-bit, switched-capacitor, successive-approximation, 11 channels, serial interface, analog-to-digital converter. The TLC2543 has an on_chip 14 channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion output goes high to indicate that conversion is complete. TLC2543 features differential high-impedance inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range. While at full samples rate, the analog input signal source impedance should be less than 50Ω and capable of slewing the analog input voltage into a 60 pF capacitor. The full scale ADC reading 0-4095 is valid in the voltage range 0-2.5V.

The ADC uses three control inputs (/CS=P27/P22; CLK=P24; DIN=P25) and is designed for communication with a host through a serial tri-state output(DOUT=P26).

If P27 is low, the V104-ADC will have output on P26. If P27 is high, the V104-ADC is disabled.

If P22 is low, the A-Drive-ADC will have output on P26. If P22 is high, the A-Drive-ADC is disabled. P22 and P27 is pulled high by 10K resistors on board.

The analog signal inputs of A0 to A10 on the terminal blocks T1 are buffered by the signal conditional operational amplifiers. and routed to A-Drive ADC U12.

The analog signal inputs of A10+ to A19+ on the terminal blocks T2 are buffered by resistor network RP22, RP23, and RP24 (default=2K). You may install offset/landing resistors at H6 and H7.

Both ADCs are using 2.5V reference. The on-board temperature sensor output V0 is directly routed to V104-ADC.

You may read the V104 ADC with the function in the library: *ce_ad12(ch);*

You may read the A-Drive ADC with the function in the library: *ad_ad12(ch);*

3.6 DAC

There are two DAC chips, one is on the V104™(U12) and one is on the A-Drive™(U13). The 12-bit DAC(MAX537) combines four 12-bit, voltage output digital to analog converters and four precision output amplifiers in a 16 pin chip. The MAX537 operates with ±5V power supply. Each DAC has a double-buffered input. A 16-bit serial word is used to load data into input/DAC register. The DACs features power-on reset, 3µs output setting time and 5 V/µs slew rate.

The V104™ uses P20=/LD, P21=DAC /CS, P24=SCLK, and P25=SDI to operate the V104 DAC. The A-Drive™ uses GND=/LD, P06=DAC /CS, P24=SCLK, and P25=SDI to operate the A-Drive DAC. The REF+ of the MAX537 is 2.5V provided by U22. The DAC requires -5V to operate. The valid DAC output

voltage range is 0-2.5V. There are Ops(U7, U8) for conditioning DAC voltage output to either current or voltage. If jumpers are on the H3, the DAC outputs current. If no jumper is on the H3, output voltage.
You may write the V104-DAC with the function in the library: *v104_da12(ch, dat);*
You may write the A-Drive-DAC with the function in the library: *ad_da12(ch, dat);*

3.7 Temperature sensor and reference voltage

A precision temperature sensor (U9, LT1025, 10 mV/Cº) is located to the screw terminals for thermocouple cold junction. The LT1025 outputs a voltage linear to degree C. While the board temperature is 25 C°, the LT1025 outputs VO=250 mV. VO is routed to the V104 ADC channel 10. See Linear Technology LT1025 data sheets for more details.
A 2.5V precision voltage reference (U22, LT1019, 3 ppm/C°) is on board providing 2.5 V reference for all ADC and DACs.

3.8 RS-232 and RS-485 Serial ports

There are two RS-232 channels routed at J4 (SER1) and J5 (SER0). J5(SER0) is the default debug port.
The SCC2691 UART is routed to the RS-485 driver U23 and header H8.

3.9 Schmitt Trigger, Counter and External Interrupt Inputs

There are 2 16-bit counters and 3 external interrupt inputs on the V104™. Schmitt-trigger inverters are provided on the A-Drive™ for high speed counter and interrupt inputs, to increase noise immunity and transform slowly-changing input signals to fast-changing and jitter-free signals. The counter and interrupt inputs are routed at H9 header. The P23=CNT1 is shared with RS-485 driver enable. The P20 is not directly connecting. Additional wiring is required.

3.10 Terminals and Power Supplies

A total of 60 positions of screw terminals are installed. Please refer to the attached A-Drive™ schematics for detail pin names.
The power supply for the A-Drive™ can be 24V or 12V. For the 24V version, a 7812 regulator must be installed in U25. The 12V version, the 7812 is not installed shorted by a wire.
The regulated voltages of +5V, -5V, +12V, -12V, +2.5V, +7V, LT1025 output VO, and LT1019 temp output are all routed to H10.

3.11 Solenoid Drives or Comparator inputs

Seven lines of high voltage driver outputs (ULN2003, U14) are capable to sink upto 350 mA at 50V. They are routed to T2 HV1 to HV7. A 8-bit address latch U11 74HC259 is used to latch the high voltage output value from V104™. You may control the high voltage driver output with *ad_hv(ch);*
The maximum power dissipation allowed is 2.20 W per chip at 25 degree C. The common substrate G is routed to T2 pin 2 via J11 1-3. The pin 4 of J11(GK) should be connected the highest positive voltage in the solenoid system with inductive load. All currents sinking in must be return from T2 pin 2=GND. A heavy gage(20) wire must be used to connect T2 GND terminal to external power supply ground return. J11 GK is connecting to the ULN2003 internal protection diodes. GK should be tied to highest voltage in the external load system. It has been connected to +24VI on board via J11 pin 2-4. ULN2003 is a sinking driver, not a sourcing driver. A typical application wiring is shown below.

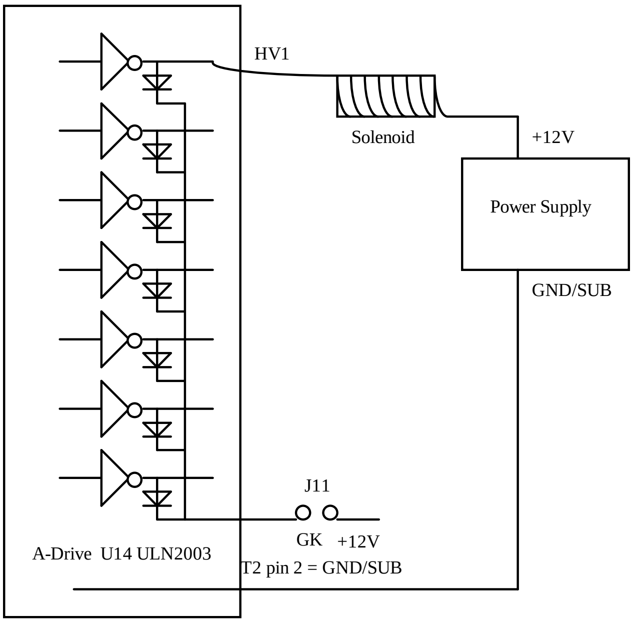


Fig. 3.7 Drive inductive load with high voltage/current drives.

If you do not need solenoid driver. You may use V25 comparator inputs without installing the U11and U14. The HV1-7 from the T2 terminals can be connected to PT1-PT7 by wire or resistors in U14 socket.

Chapter 4
Software

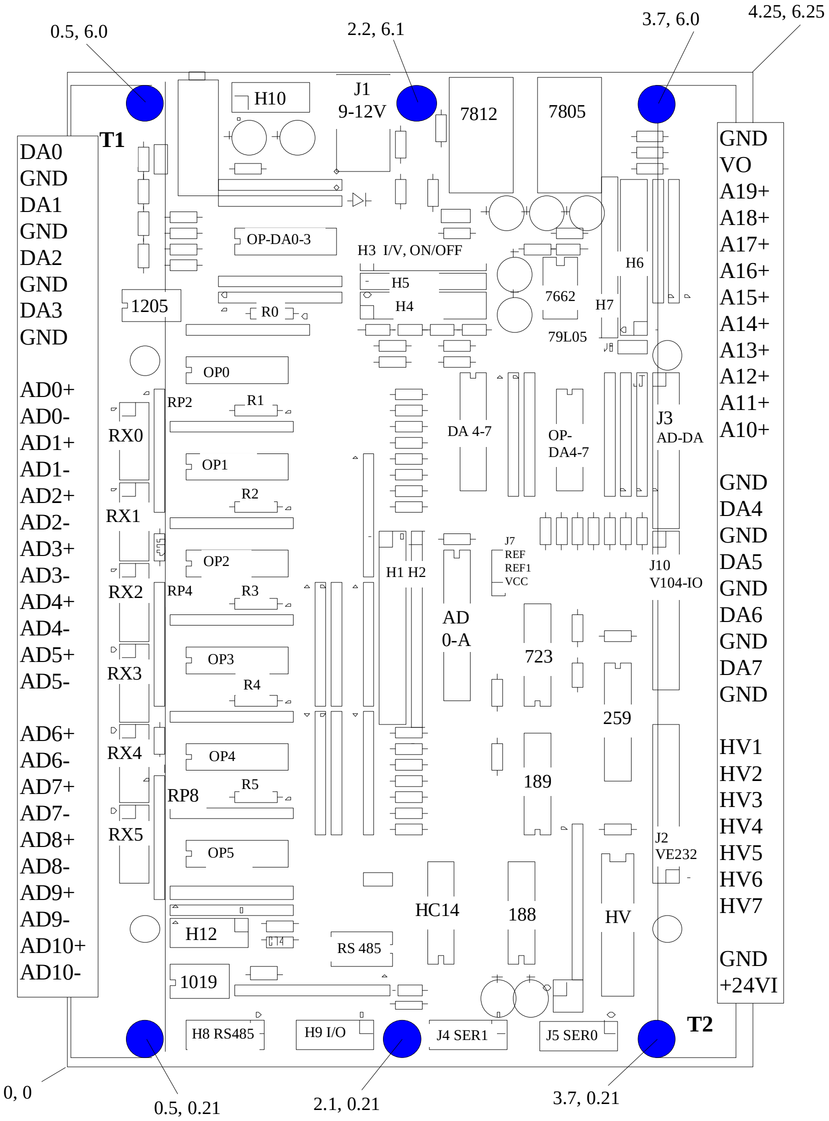
Please refer to the V104™ Technical Manual and the V25 User's Manual for more details.

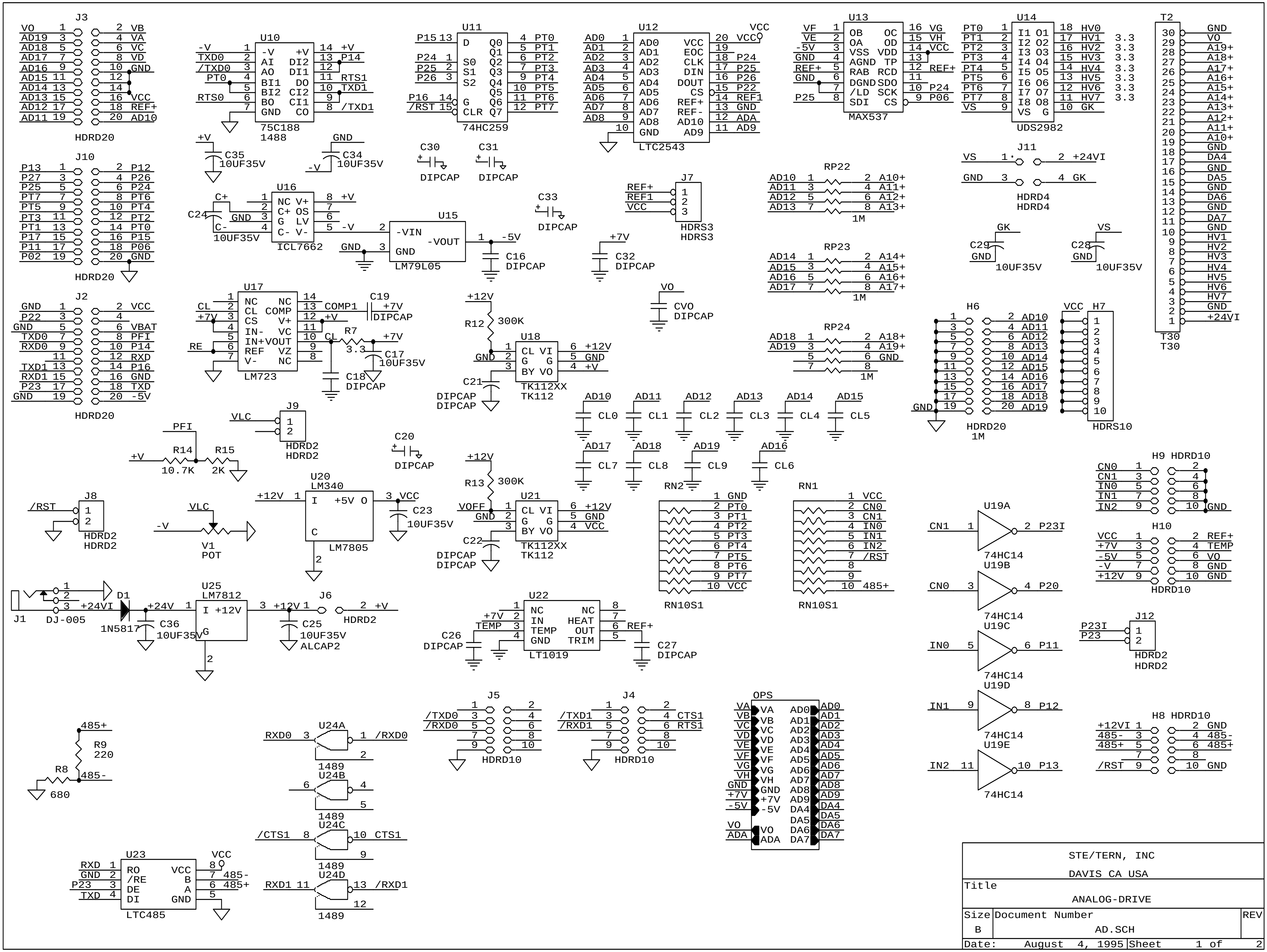
Functions in AD.LIB Library:

```
//*******************************************************
// P0, P1, P2 initialization for the Analog-Drive. 06-25-95
//        P03=HWD, P05=LED, P06=DAC-CS
//        P15=HV-D, P16=HV-G
//        P20,P21,P22,P23,P24,P25,P26,P27 output high
//*******************************************************
void ad_init(void);

/*****************************************************
        void ad_da12(char c, int dat)
        output 12-bit dat to U13 DAC channel "c" of AIO
        where c = 0 to 3
                dat=0-4095
        P06=CS,P05=LED,P03=HWD output
        P23=EN485,P24=CLK,P25=DIN,P26=ad_DOUT,P27=ad_CS
*****************************************************/
void ad_da12(char c, int dat);


/*******************************************************
//        ad_ad12.c
//        Analog to Digital conversion using U12 TLC2543 on the A-Drive        06-25-1995
//        Input:
//                unsigned char c = input channel
//                c = 0,    input ch = AD0
//                c = 1,    input ch = AD1
//                c = 2,    input ch = AD2
//                c = 3,    input ch = AD3
//                c = 4,    input ch = AD4
//                c = 5,    input ch = AD5
//                c = 6,    input ch = AD6
//                c = 7,    input ch = AD7
//                c = 8,    input ch = AD8
//                c = 9,    input ch = AD9
//                c = a,    input ch = AD10
//                c = b,    input ch = (vref+ - vref-) /2
//                c = c,    input ch = vref-
//                c = d,    input ch = vref+
//                c = e,    software power down
//        There are 2 ADCs on the A-Drive: 1 on V104(P27) and 1 on A-Drive(P22)
//        In order to operate ADC, P22, P24, P25, P27 must be output
//                P22 and P27 must be only one low at a time, and P26 must be input.
//                Before enter the ce_ad12 or ad_ad12 You need to define P2 as:
//                I/O function with PMC2=0x00, PM2=0xc3
//        pokeb(0xfff0,0x12,0x00);// PMC2=0x00, all pins are I/O function
//        pokeb(0xfff0,0x11,0xc3);// P22=CS,P23=485,P24=CLK,P25=DIN,P26=DOUT
```

```
//
//          Output: 12 bit AD data of the previous channel !
//                  Unipolar:
//                  (Vref+ - Vref-)=0x7ff
//                  Vref- = 0x000
//                  Vref+ = 0xfff
//
//          Use 1 wait state for Memory and I/O without RDY, < 300 us execution time
//          Use 0 wait state for Memory and I/O with VEP010, < 270 us execution time
*****************************************************************/
int ad_ad12(unsigned char c);


//*****************************************************************
//          void ad_hv(int ch, int k);
//          U11 74HC259 and U14 HV control for the Analog-Drive        06-25-95
// ch = 0-7, k=0/1
// P15=D, P16=CS, P24, P25, P26 all output.
//          P22, P27 must high disable ADCs DOUT
//*****************************************************************
void ad_hv(int ch, int k);
```

Appendix A: Layout of the Analog-Drive™





STE/TERN, INC

DAVIS CA USA

Title

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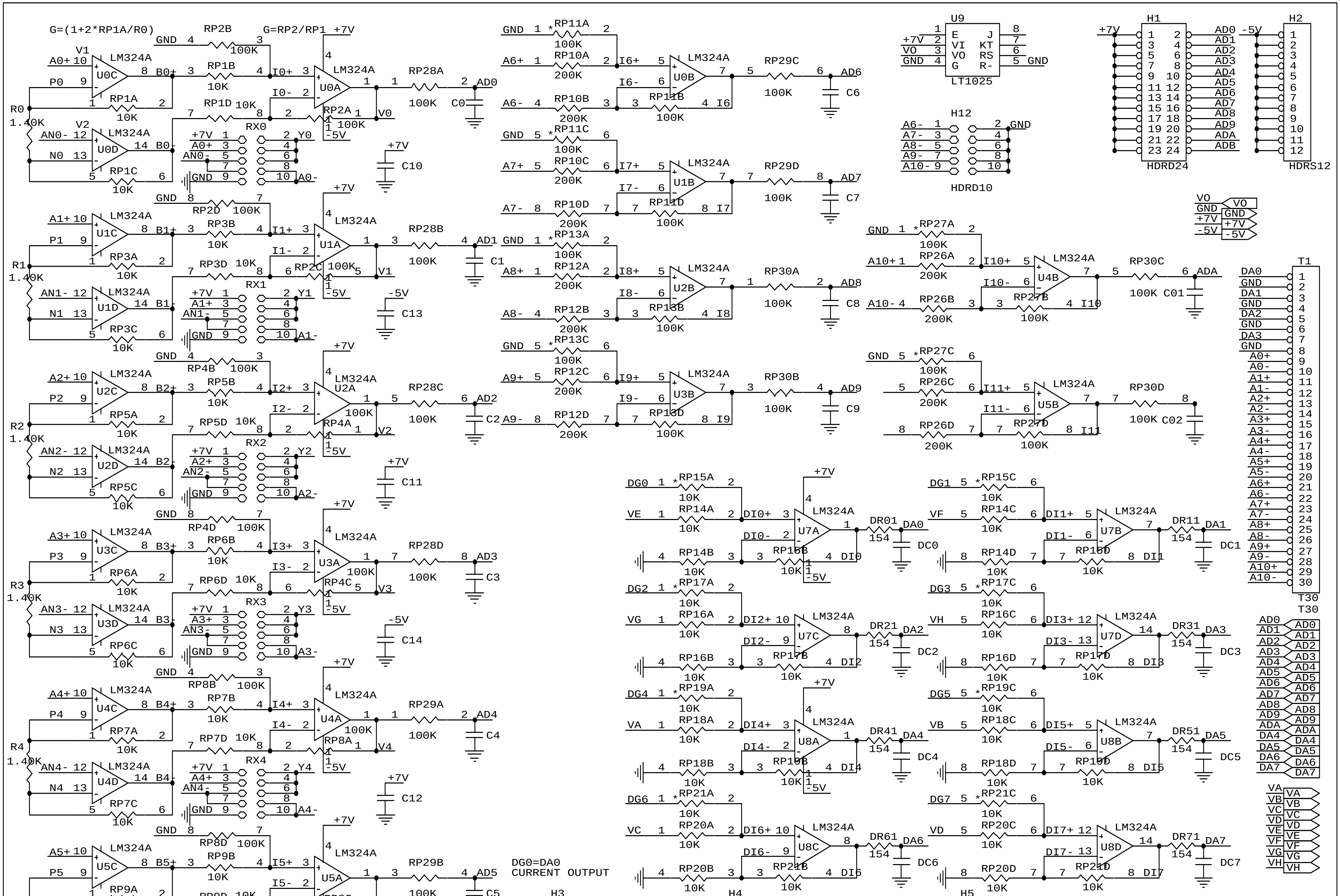

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