# A104STM

16-bit microcontroller with 7 Serial Ports, 80+ I/Os, ADC, DAC, Solenoid Drivers and LCD interface Based on the 40MHz 188 CPU



# Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

## 1.1 Introduction

The *A104*S is a 16-bit microcontroller based on the original *A104* design. Measuring 4.0 by 3.6 by 0.5 inches, the *A104*S offers a complete C/C++ programmable computer system with a 16-bit, high performance CPU (188), operating at 40 MHz system clock with zero-wait-state. The *A104*S supports 24 TTL bi-directional I/O pins, seven TTL outputs, 11 channels of 12-bit ADC, two channels of 12-bit DAC, six channels RS-232 and one channel RS485, a real-time clock, battery backup, watchdog timer, PWM, three timer/counters, a 512-byte serial EEPROM, up to 512 KB SRAM, and up to 512 KB ROM/Flash.

The *A104S* is designed for control applications that require precision analog conversion, solenoid drivers, and high-speed performance. The *A104S* is designed with a 64-pin header which is based upon PC104 standard, routing common signals such as data/address bus, interrupt lines, VCC, and GND to the header, yet it is not 100% PC104 compatible. While some customers have integrated the *A104S* into PC104 applications, TERN does not guarantee compatibility or provide technical support for PC104 applications.

Two asynchronous serial ports from the 188 CPU support reliable DMA-driven serial communication at up to 115,200 baud with RS-232 drivers. In addition, two dual UARTs SC26C92 (RS-232) are installed on-board to give a total of 6 RS-232 channels. An optional UART SCC2691 can be installed using an RS-485 driver for a seventh asynchronous serial port.

An optional real-time clock provides information on the year, month, date, hour, minute, and second and an interrupt signal.

Three 16-bit programmable timers/counters are on board. Two timers can be used to count or time external events, up to 10 MHz, or to generate non-repetitive or variable-duty-cycle waveforms as PWM outputs. Pulse Width Demodulation (PWD), a distinctive feature, can be used to measure the width of a signal in both its high and low phases. It can be used in many applications, such as bar-code reading. The 32 I/O pins on the 188 CPU are multifunctional and user-programmable. You may have 15 or more lines free to use, depending on your application and which optional hardware is installed.

The 82C55 I/O chip on-board provides an additional 24 bi-directional I/O lines, of which 14 TTL user-definable I/O lines can be used to interface to a graphic- or character-type LCD and a keypad. An adjustable negative voltage (-10V) may optionally be installed on-board for LCD contrast.

A supervisor chip (691) provides power fail detection, reset, and a watchdog timer. The optional 12-bit ADC has 11 channels of analog inputs with sample-and-hold and a high-impedance reference input. The ADC conversion rate is up to a sample rate of 10 KHz. One DAC chip may be installed on-board to provide two channels 12-bit, 0-4.095V analog voltage outputs capable of sinking or sourcing 5 mA.

By default, a 5V linear regulator (8.5-12V DC input) is installed. A 5V switching regulator (up to 35V DC input) may be installed to reduce power consumption and heat. The switching regulator introduces more noise than a linear regulator.

The FlashCore-0 expansion card may be installed to provide memory expansion via CompactFlash (up to 2GB). In addition, the MemCard-B expansion card may be installed to add an additional 33 12-bit ADC, 6 24-bit ADC, 2GB memory, and an Ethernet interface.

#### **Features:**

#### Standard Features

- Dimensions: 4.0 x 3.6 x 0.5 inches
- Easy to program in C/C++
- Power consumption: 160/120/60 mA at 9/12/24V
- Power input: +8.5V to +12 V unregulated DC with linear regulator
  - or, +8.5 to +35V unregulated DC with switching regulator (optional)
- Temperature:  $-40^{\circ}$ C to  $+80^{\circ}$ C

- 16-bit CPU (188), Intel 80x86 compatible, 40 MHz
- High performance, zero-wait-state operation at 40 MHz
- 128KB SRAM, Up to 512KB Flash/ROM
- 2 high-speed PWM outputs and Pulse Width Demodulation
- 2 SCC2692 dual UARTs with RS-232 drivers
- 24 additional bi-directional I/O lines from 82C55
- 512-byte serial EEPROM
- 6 external interrupt inputs, 3 16-bit timer/counters
- 2 CPU serial ports
- Supervisor chip (691) for power failure, reset and watchdog
- 7 TTL outputs plus 14 TTL I/Os for Graphic/character LCD or keypad interface
- Up to 20 MB memory expansion with PCMCIA via the MemCard-A

#### **Optional Features:**

- 512KB SRAM
- 11 channels of 12-bit ADC, sample rate up to 10 KHz (TLC2543)
- 2 channels of 12-bit DAC (LTC1446), 0-4.095V output
- SCC2691 UART with RS-485 drivers
- Real-time clock RTC72423, lithium coin battery
- Precision reference, 20 PPM/°C, 5V
- LCD negative voltage port
- 68-pin connector based upon PC104 standard

### 1.2 Hardware

#### **UART SCC2692**

The two dual UARTs (SCC2692, Signetics, U16 and U17) are 44-pin PLCC chips. U16 is mapped into the I/O address space at **0x300**, and U17 is at **0x200**. The SCC2692 includes two independent full-duplex asynchronous receiver/transmitters, a quadruple buffered receiver data register, an interrupt control mechanism, programmable data format, selectable baud rate for the receiver and transmitter, a multifunctional and programmable 16-bit counter/timer, an on-chip crystal oscillator, and a multi-purpose input/output including RTS and CTS mechanism.

A 3.6864 MHz external crystal can be installed as the default crystal for the dual UART.

For more detailed information, refer to the SCC2692 data sheets (TERN installation CD, \text{\text{tern\_docs\parts\scc2692.pdf}}).

Only RS-232 drivers are provided for the dual UARTs. The RS-232 signals are routed to the P2 header.

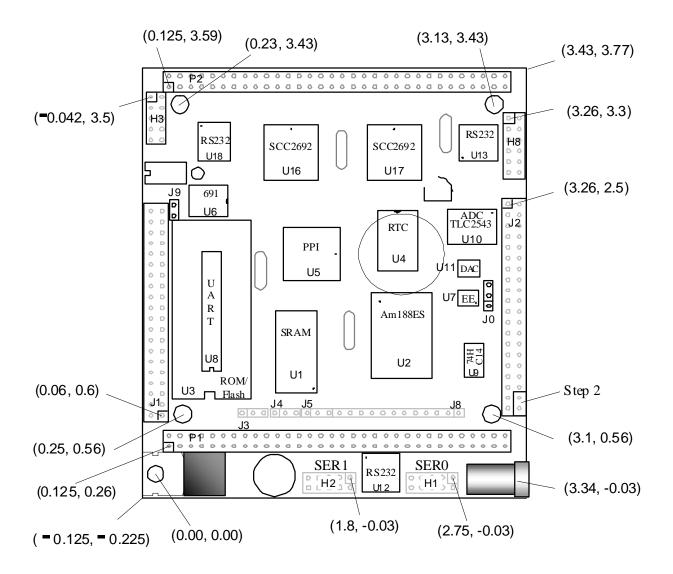
Sample programs for the A104S are included in the a104s.ide and ae.ide project file found in the c:\tern\186\samples\ae directories, respectively.

The A-Engine technical manual (\tern\_docs\manuals directory) will provide all other relevant information. In addition, sample code found in the \tern\186\samples\ae directory gives examples for the CPU.

# A104S Layout

## **September 6, 2000**

The A104S measures 4.0 x 3.6 inches. All dimensions shown below are in inches.



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