B-Engine™

±10V Bipolar Simultaneous Sampling ADC, DAC, Ethernet and CompactFlash

Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

The ***B-Engine™*** (***BE***) is a high performance, low cost, C/C++ programmable controller with ±10V bipolar analog inputs. It is intended for networked industrial process control, power-line monitoring and protection, multiphase motor control, high-speed data acquisition. With its high reliability and low cost, it is ideal for industrial OEM applications.

A true bipolar, simultaneous sampling ADC (AD7606, 16-bit or AD7607, 14-bit) can be installed on the ***BE***. The ADC can accept ±10V or ±5V true bipolar analog signals while sampling at throughput rates up to 200 kSPS for all 8 analog inputs. Each analog input contains second-order antialansing filter, sample-and-hold amplifier and clamp protection tolerant up to ±16.5V. With 1M ohm analog input impedance, a 7000V ESD rating, and sustaining up to ±10 mA input current, the analog inputs are designed to survive in a rough industrial environment. The ***BE*** allows *simultaneous* sampling on all eight analog inputs. Via 16-bit parallel interface, DMA operation can transfer 8 16-bit data into RAM or CompactFlash cards with low software overhead.
A 4 channel, 16-bit DAC(DAC8544) can be installed. Its on-chip output amplifier allows rail-to-rail voltage output (0-5V). It connects to the host CPU via high speed 16-bit parallel interface.
A Fast Ethernet Module can be installed to provide 100M Base-T network connectivity. This Ethernet module has a hardware LSI TCP/IP stack. It implements TCP/IP, UDP, ICMP and ARP in hardware, supporting internet protocol DLC and MAC. The hardware Ethernet module releases internet connectivity and protocol processing from the host processor, which represents a huge improvement over software-based TCP/IP stacks. The resulting system can easily handle transmissions in the 100KB/s+ range in real world applications.
The ***BE*** supports up to 32 GB mass storage CompactFlash cards in raw data mode; it also supports a Windows compatible FAT16 file system (up to 2GB), allowing user easily transfer data.
The ***BE*** features 16-bit ACTF Flash (256 KW) and battery-backed SRAM (256 KW). It also includes 3 timers, PWMs, 20+ PIOs, 512-byte serial EEPROM, two UARTs, 3 timer/counters, and a watchdog timer. PIO pins are multifunctional and user programmable. A real time clock (RTC27423, Epson) is available.
The ***BE*** is powered via regulated 5V. The ***BE*** works with most TERN expansion boards including the B48, V232, P52, P100, and P300. The V232 can provide RS232 drivers and regulated 5V
The ***B48™*** is an expansion board supporting 6 AD7606/7 chips to provide additional up to 48 analog inputs per board. Multiple B48 can be stacked.

The *BE* is an ideal upgrade for the A-Engine, V25-Engine, 386-Engine, or R-Engine providing increased reliability, networking functionality, and performance. They have the similar mechanical dimensions, pin outs, software drivers, and both are programmed using Paradigm C++ TERN Edition Evaluation Kit (EV-P) or Development Kit (DV-P).

The ***BE*** can be integrated into an OEM product as a processor core component. It also can be used to build a smart sensor, or can act as a node in a distributed microprocessor system.

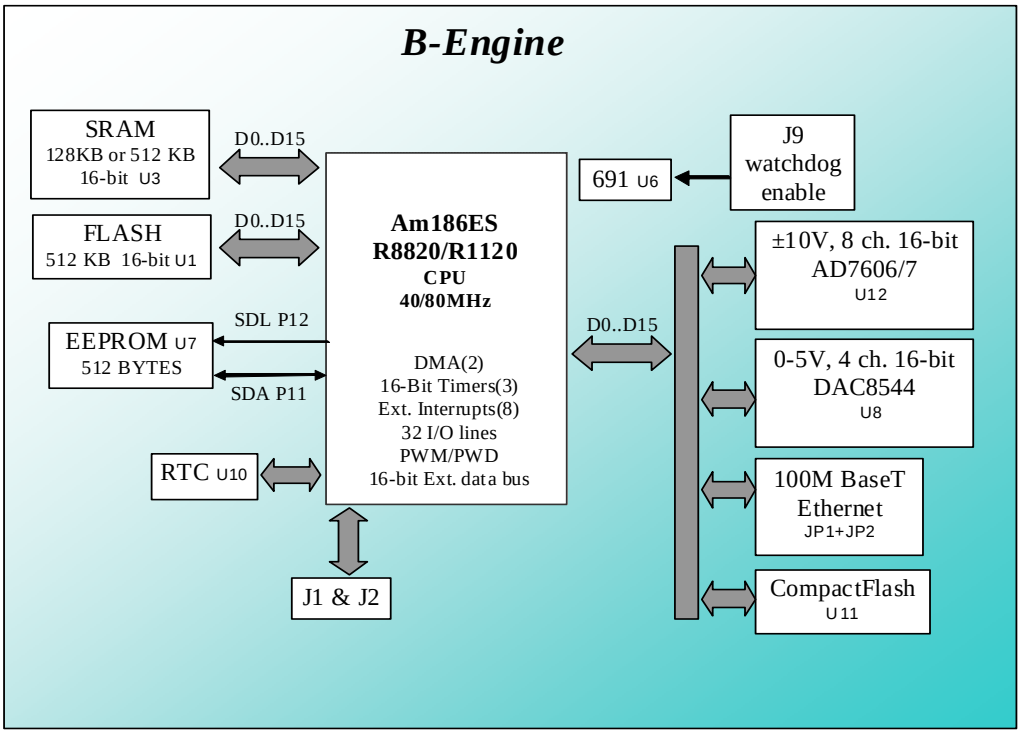


Figure 1.1 Functional block diagram of the E-Engine

The ***BE*** supports on-board 512 KB 16-bit Flash and up to 512 KB 16-bit battery-backed SRAM. The on-board ACTF Flash has a protected boot loader and can be easily programmed in the field via serial link. Users can download a kernel into the Flash for remote debugging. With the DV-P Kit support, user application codes can be easily field-programmed into and run out of the Flash.

A 512-byte serial EEPROM is included on-board. Two DMA-driven serial ports from the Am186ES support high-speed, reliable serial communication at a rate of up to 115,200 baud. All serial ports support 8-bit and 9-bit communication.

There are three 16-bit programmable timers/counters and a watchdog timer. Two timers can be used to count or time external events, at a rate of up to 10 MHz, or to generate non-repetitive or variable-duty-cycle waveforms as PWM outputs. Pulse Width Demodulation (PWD), a distinctive feature, can be used to measure the width of a signal in both its high and low phases. It can be used in many applications, such as bar-code reading.

The ***BE*** *has* 32 user-programmable, multifunctional I/O pins from the CPU. Schmitt-trigger inverters are provided for six external interrupt inputs, to increase noise immunity and transform slowly-changing input signals into fast-changing and jitter-free signals. A supervisor chip with power failure detection, a watchdog timer, an LED, and expansion ports are on-board.

Features:

- 3.6 x 2.3 x 1”, 200 mA at 5V
- 40 or 80 MHz, 16-bit CPU, program in C/C++
- 256 KW 16-bit Flash, 256 KW 16-bit SRAM, 512 bytes EE
- 20+ TTL I/Os, Real-time clock, 2 serial ports, PWM, counters
- 8 ch ±10V Bipolar Simultaneous Sampling ADC (AD7606/7)
- 4 ch 0-5V Rail-to-Rail DAC (DAC8544)
- Hardware TCP/IP stack for 100M Base-T Ethernet
- CompactFlash card with FAT file system support

1.2 Physical Description

The physical layout of the B-Engine is shown in Fig 1.2.

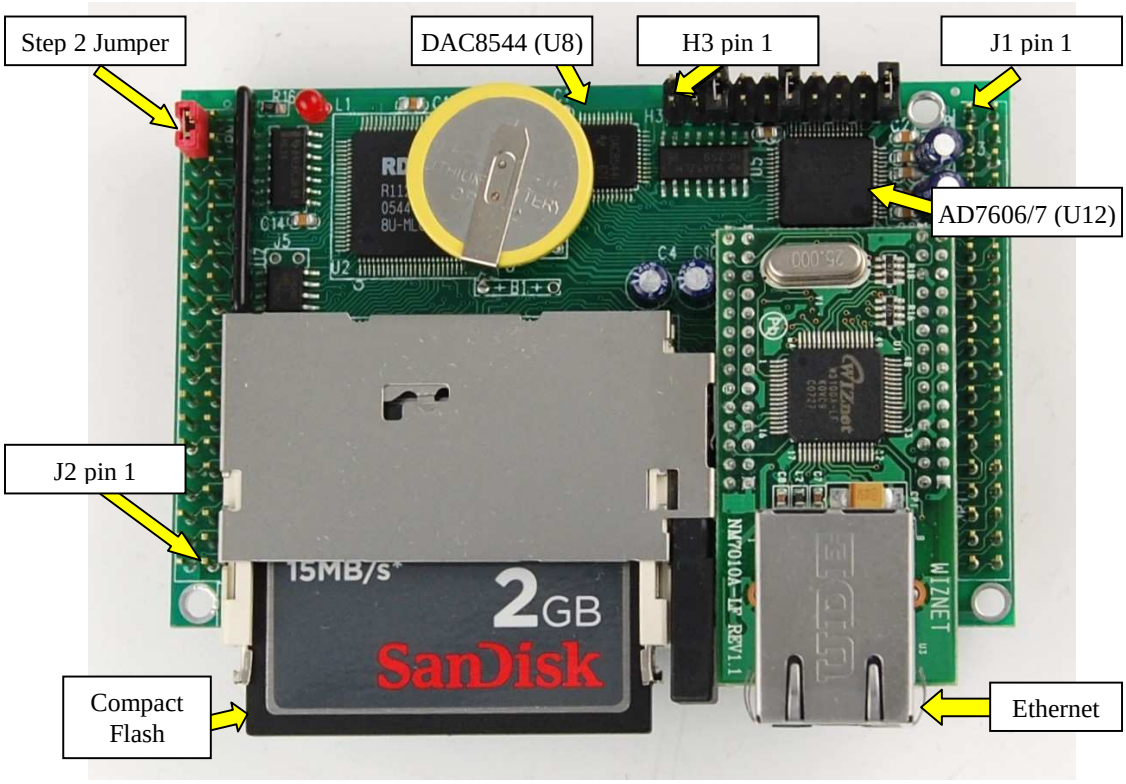


Figure 1.2 B-Engine

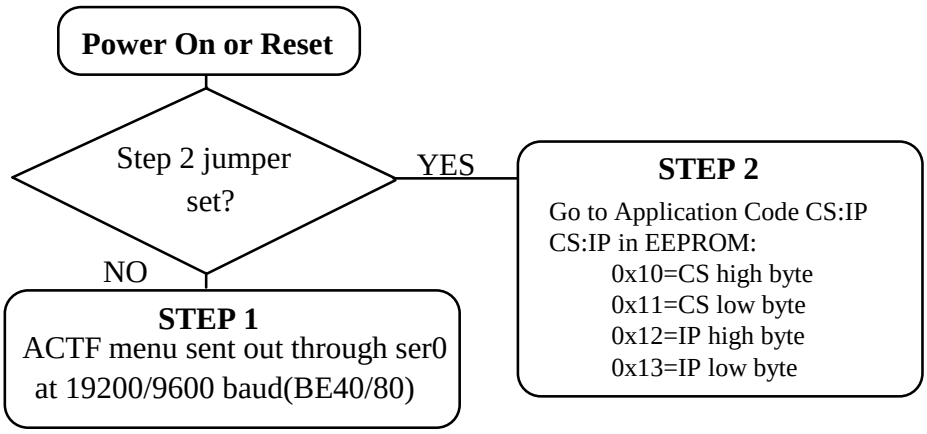


Figure 1.3 Flow chart for ACTF operation

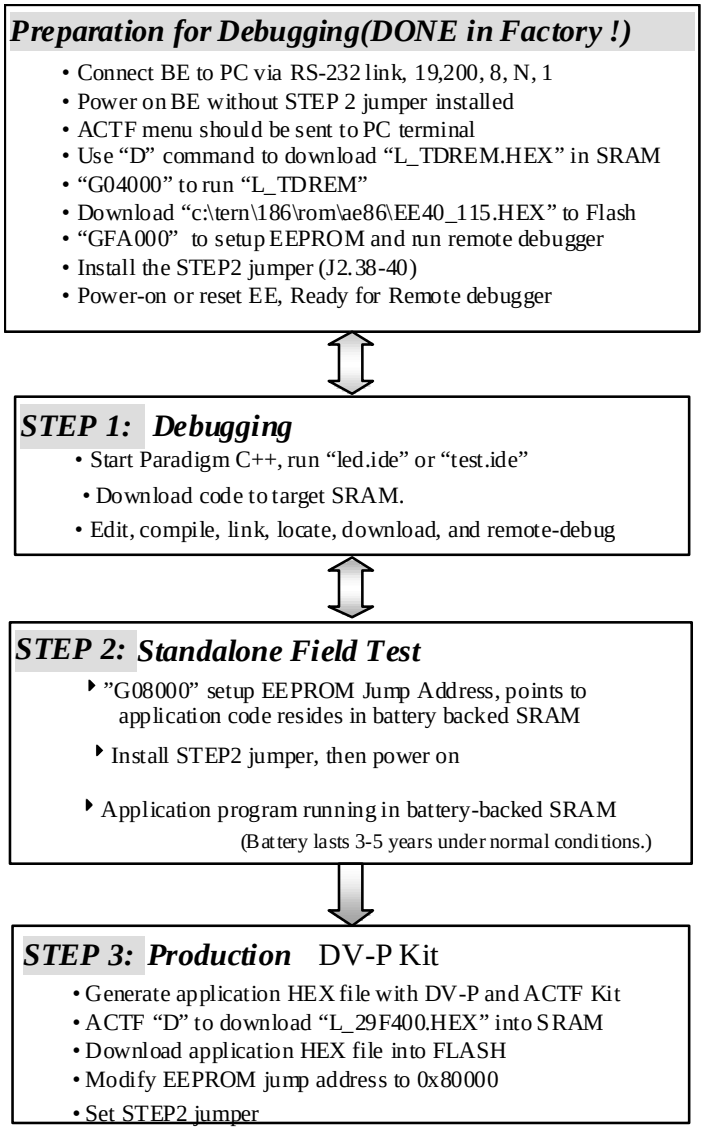
The "ACTF boot loader" resides in the top protected sector of the 512KB on-board Flash chip (29F400).

By default, in the factory, before shipping, the DEBUG kernel (EE40_115.hex or EE80_115.hex) is pre-loaded in the Flash starting at 0xFA000, and the RED STEP2 jumper is installed, ready for Paradigm C++ debugger. User does not need to download a DEBUG kernel to start with.

At power-on or RESET, the "ACTF" will check the STEP 2 jumper. If STEP 2 jumper is not installed, the ACTF menu will be sent out from serial port0 at 19200 baud for a BE40, or 9600 baud for a BE80.
If the STEP 2 jumper is installed, the "jump address" located in the on-board serial EE (see App. B) will be read out and then jump to that address. A DEBUG kernel "EE40_115.hex" for the BE40 or "EE80_115.hex" for the BE80 can be downloaded, residing in "0xFA000" of the 512KB on-board flash chip.
The "EE40_115.hex" can also be downloaded into an BE80 for easier running all demo projects, which are designed for running 40MHz.

1.3 B-Engine Programming Overview

Steps for product development:



The user's application program must reside in SRAM for debugging in STEP1, reside in battery-backed SRAM for the standalone field test in STEP2, and finally be programmed into Flash for a complete product. For production, the user must produce an ACTF-downloadable HEX file for the application, based on the DV-P Kit. The "STEP2" jumper (J2 pins 38-40) must be installed for every production-version board.

Step 1 settings

In order to talk to BE with Paradign C++, the BE must meet these requirements:

1) EE40_115.HEX or EE80_115.HEX must be pre-loaded into Flash starting address 0xfa000.

2) The SRAM installed must be large enough to hold your program.

For a 32K SRAM, the physical address is 0x00000-0x07fff
For a 128K SRAM, the physical address is 0x00000-0x01ffff
For a 512K SRAM, the physical address is 0x00000-0x07ffff

3) The on-board EE must have a Jump Address for the EE40_115.HEX or EE80_115.HEX with starting address of 0xfa000.

4) The STEP2 jumper must be installed on J2 pins 38-40.

For further information on programming the E-Engine, refer to the manual on the TERN CD under: tern_docs\manuals\development kit pro.pdf.

The ***BE*** works with most TERN expansion boards including the B48, P50, P100, P300, MotionC, and MMC.

Figure 1.4 B-Engine with VE232, Compact flash and Ethernet

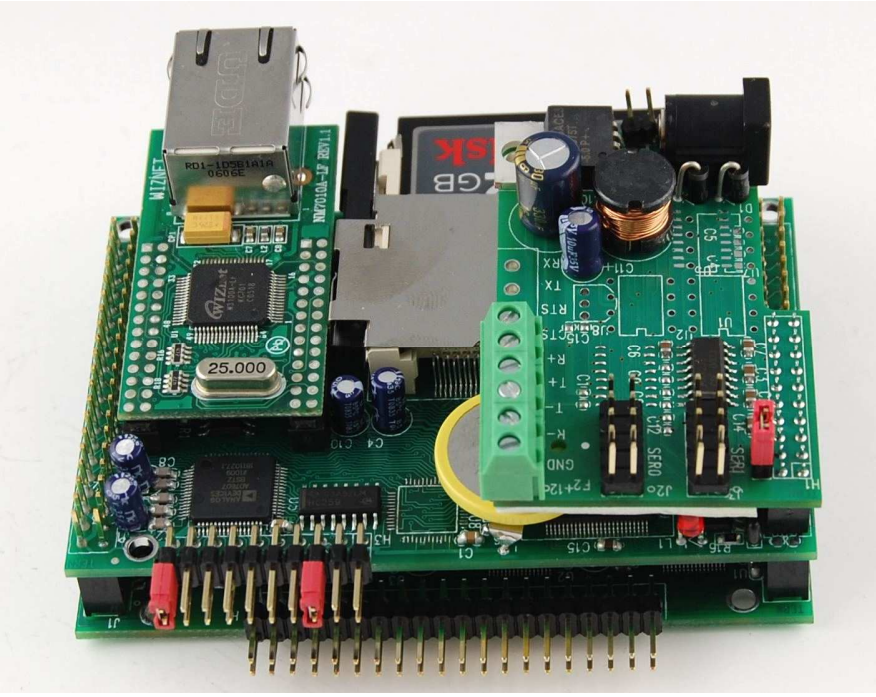


Figure 1.5 B-Engine with B48, VE232, Compact flash and Ethernet

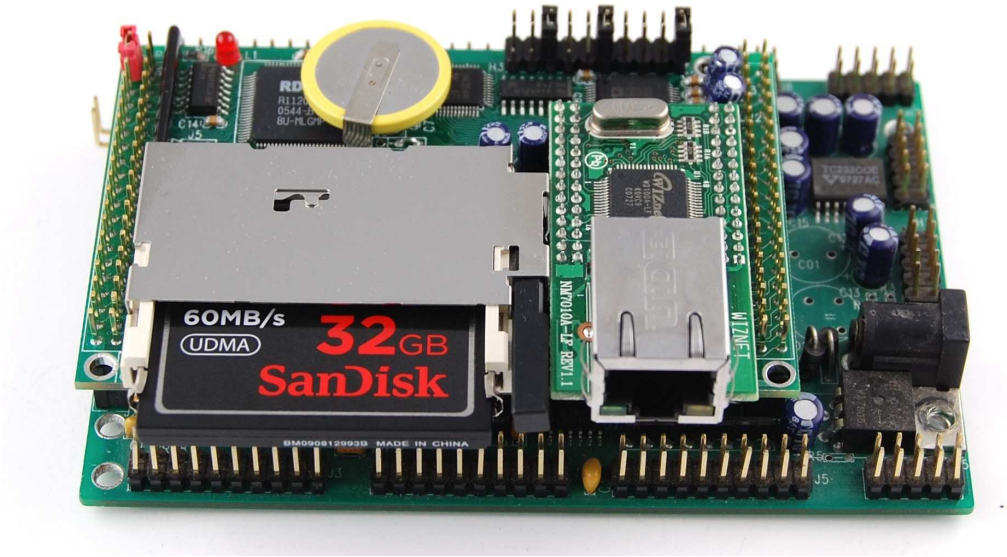


Figure 1.6 B-Engine with P100, Compact flash and Ethernet

Chapter 2: Installation

2.1 Software Installation

Please refer to the "development kit pro.pdf" technical manual on the TERN installation CD, under tern_docs\manual\ development kit pro.pdf, for information on installing software.

2.2 Hardware Installation

Overview

- Connect PC-IDE serial cable:
  For debugging (STEP 1), place IDE connector on SER0 (H1) with red edge of cable at pin 1. This DEBUG cable is a 10-pin IDE to DB9 cable, made by TERN (See Appendix D).
- Connect wall transformer:
  Connect 9V wall transformer to power and plug into power jack using power jack adapter supplied with EV-P/DV-P Kit

Hardware installation consists primarily of connecting the microcontroller to your PC.

2.2.1 Connecting to the PC

The following diagram (Fig 2.1) provides the location of the debug serial port and the power jack. The controller is linked to the PC via a serial cable (DB9-IDE) which is supplied with TERN's EV-P / DV-P Kits.

The controller communicates through SER0 by default. Install the 5x2 IDE connector on the SER0 5x2 pin header. ***IMPORTANT:*** *Note that the* ***red*** *side of the cable must point to pin 1 of the SER0 header.* The DB9 connector should be connected to one of your PC's COM Ports (COM1 or COM2).

2.2.2 Powering-on the BE™

By factory default setting:
1) The RED STEP2 Jumper is installed. (Default setting in factory)
2) The DEBUG kernel is pre-loaded into the on-board flash starting at address of 0xFA000. (Default setting in factory)
3) The EEPROM is set to jump address of 0xFA000. (Default setting in factory)

Connect +9-12V DC to the DC power terminal. The DC power jack adapter is center negative.

The on-board LED should **blink twice and remain on**, indicating the debug kernel is running and ready to communicate with Paradigm C++ TERN Edition for programming and debugging.

(See next page for connection diagram).

2.2.3 Connecting the BE™ via VE232

The proper connections required to debug the board (through Paradigm software). J2 (SER 0) is a 5x2 pin header on the VE232.

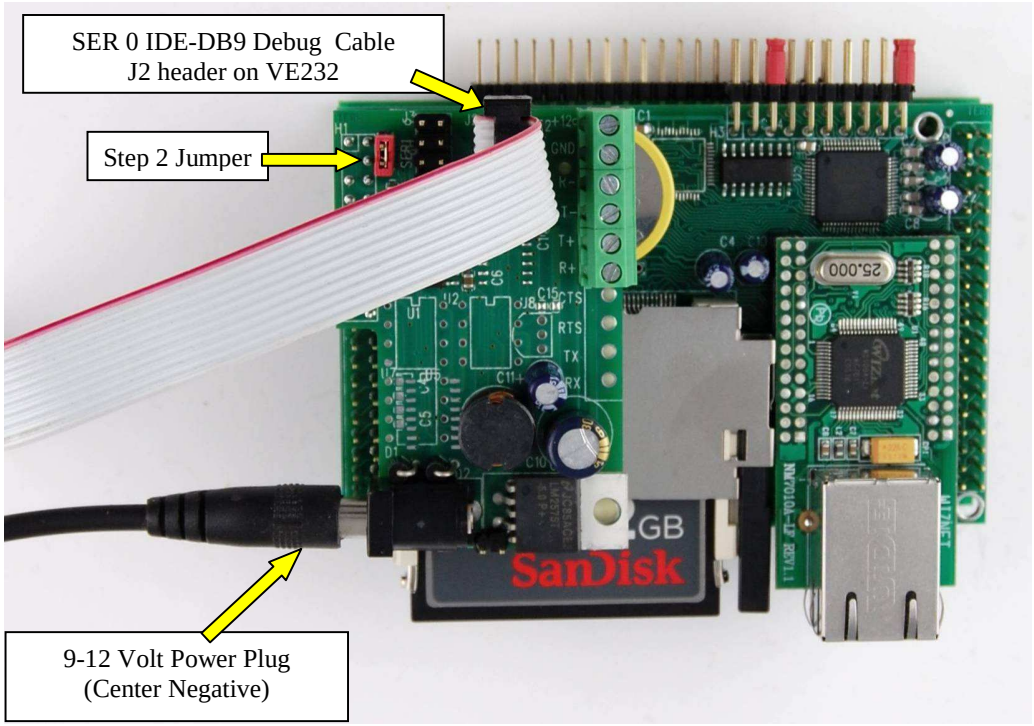


Figure 2.1: BE+VE232 with Debug Cable (Ser0), Power Plug, and Step 2 Jumper shown

NOTE: Remember to watch for the "**double blink**" off the LED. This indicates the **Debug Kernel** has been loaded with the **jump address** pointing to it. This is mandatory to commence downloading code through the Paradigm environment.

Chapter 3: Hardware

3.1 Am186ES/R8820/R1120 - Introduction

The Am186ES is based on industry-standard x86 architecture. The Am186ES controllers uses 16-bit external data bus, are higher-performance, more integrated versions of the 80C188 microprocessors which uses 8-bit external data bus. In addition, the Am186ES has new peripherals. The on-chip system interface logic can minimize total system cost. The Am186ES has two asynchronous serial ports, 32 PIOs, a watchdog timer, additional interrupt pins, a pulse width demodulation option, DMA to and from serial ports, a 16-bit reset configuration register, and enhanced chip-select functionality.

R8820 is a drop-in replacement 5V, 40MHz chip for the AM186ES. Connecting J0.1=J0.2.

R1100 is a 80MHz, 3.3V chip can be installed on the B-Engine with J0.2=J0.3.

By default, the B-Engine uses 5V 40 MHz R8820 and low power 55-70 ns SRAM with battery backup.
Optional 3.3V 80 MHz R1120 can be installed.
At 80 MHz, the low power 55 ns SRAM with battery backup works fine but will not be able to support DMA operation.
A fast 10/15/25 ns SRAM (Not low power) can be used to support zero wait state and DMA operation at 80 MHz, but the backup battery will be drain in few days.
There are three pads on the PCB for battery. One pads is ground, and the other two pads allowing a 3V backup lithium battery be installed in two different positions:
1) The battery's positive lead is installed in the pad which is away from the RTC, supporting the RTC only. No battery backup for the SRAM.
2) The battery's positive lead is installed in the pad which is closer to the RTC, supporting both RTC and SRAM.
In the future, when the fast (10 ns) and low low standby power SRAM is available, then 80 MHz B-Engine can have both RTC and SRAM with battery backup plus the DMA, zero wait state operation.
User can use sample program c:\tern\186\samples\ee\rdc_id.c to read the ID register(0xfff4), in order to identify RDC CPU type.

R1100=0xC5D9, R1120=0x85D9, R8820/30=0x04D9(xxD9)

3.2 Am186ES – Features

3.2.1 Clock and crystal

Due to its integrated clock generation circuitry, the Am186ES microcontroller allows the use of a times-one crystal frequency. The design achieves 40 MHz CPU operation, while using a 40 MHz crystal.

The system CLKOUTA signal is routed to J1 pin 4, default 40 MHz for BE40.

CLKOUTA remains active during reset and bus hold conditions. The initial function ae_init(); disables CLKOUTA and CLKOUTB with clka_en(0); and clkb_en(0);

You may use clka_en(1); to enable CLKOUTA=CLK=J1 pin 4.

The R8820 uses a 40 MHz crystal.

By default the 3.3V R1120 uses a 20 MHz crystal. The CPU speed is software programmable with the PLL.

At power-on, the on-board ACTF Flash programs the R1120 running at 20 MHz system clock, so a 9600 baud (instead 19,200 baud) is used for ACTF manu.

Two debug kernels are available:

c:\tern\186\rom\ae86\EE40_115.hex, or c:\tern\186\rom\ae86\EE80_115.hex

The EE40_115.hex will run the R1120 at 40 MHz, and the EE80_115.hex will run the R1120 at 80 MHz.

By default, the EE80_115.hex is pre-programmed for the 80 MHz B-Engine.

User can use software to setup the CPU speed:

```
outport(0xfff8,0x0103);  // PLLCON, 20MHz crystal, 0103=40 MHz, 0107=80MHz
```

3.2.2 External Interrupts and Schmitt Trigger Input Buffer

There are eight external interrupts: INT0-INT6 and NMI.

/INT0, J2 pin 8, free to use.
/INT1, J2 pin 6, free to use.
/INT2, J2 pin 19, AD7606/7 busy
/INT3, J2 pin 21, free to use
/INT4, J2 pin 33, used by 100M BaseT Ethernet
INT5=P12=DRQ0, used by B-Engine as output for LED/EE/HWD
INT6=P13=DRQ1, J2 pin 11, free to use
/NMI, J2 pin 7

Some of external interrupt inputs, /INT0, 1, 3, 4 and /NMI, are buffered by Schmitt-trigger inverters (U9, 74HC14), in order to increase noise immunity and transform slowly changing input signals to fast changing and jitter-free signals. As a result of this buffering, these pins are capable of only acting as input.

These buffered external interrupt inputs require a falling edge (HIGH-to-LOW) to generate an interrupt.

The B-Engine uses vector interrupt functions to respond to external interrupts. Refer to the Am186ES User's manual for information about interrupt vectors.

3.2.3 Asynchronous Serial Ports

The Am186ES CPU has two asynchronous serial channels: SER0 and SER1. Both asynchronous serial ports support the following:

- Full-duplex operation
- 7-bit, 8-bit, and 9-bit data transfers
- Odd, even, and no parity
- One stop bit
- Error detection
- Hardware flow control
- DMA transfers to and from serial ports
- Transmit and receive interrupts for each port
- Multidrop 9-bit protocol support
- Maximum baud rate of 1/16 of the CPU clock speed
- Independent baud rate generators

The software drivers for each serial port implement a ring-buffered DMA receiving and ring-buffered interrupt transmitting arrangement. See the samples files ***s1_echo.c*** and ***s0_echo.c***.

Important Note: For 80MHz BE80, DMA functions are not available when by default low power 55 ns SRAM is installed. If install a 25 ns SRAM, 80MHz EE can have all DMA functions, but it will drain the backup battery fast.

3.2.4 Timer Control Unit

The timer/counter unit has three 16-bit programmable timers: Timer0, Timer1, and Timer2.

Timer0 and Timer1 are connected to external pins:

Timer0 output = P10 = J2 pin 12
Timer0 input = P11 = U7 EE pin 5
Timer1 output = P1 = J2 pin 29
Timer1 input = P0 = J2 pin 20

Timer0 input P11 is used by the on-board EE and not recommended for other external use.

The timer can be used to count or time external events, or can generate non-repetitive or variable-duty-cycle waveforms.

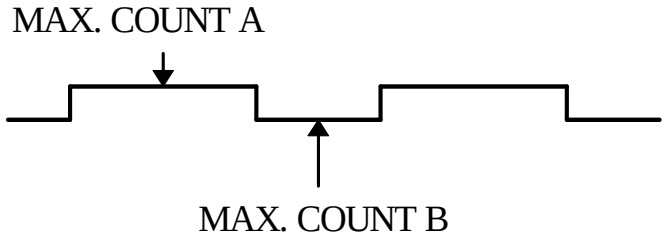
Timer2 is not connected to any external pin. It can be used as an internal timer for real-time coding or time-delay applications. It can also prescale timer 0 and timer 1 or be used as a DMA request source.

The maximum rate at which each timer can operate is 10 MHz, since each timer is serviced once every fourth clock cycle. Timer output takes up to six clock cycles to respond to clock or gate events. See the sample programs ***timer02.c*** and ***ae_cnt1.c*** in the **`tern\186\samples\ae`** directory.

3.2.5 PWM outputs and PWD

The Timer0 and Timer1 outputs can also be used to generate non-repetitive or variable-duty-cycle waveforms. The timer output takes up to 6 clock cycles to respond to the clock input. Thus the minimum timer output cycle is 25 ns x 6 = 150 ns (at 40 MHz).

Each timer has a maximum count register that defines the maximum value the timer will reach. Both Timer0 and Timer1 have secondary maximum count registers for variable duty cycle output. Using both the primary and secondary maximum count registers lets the timer alternate between two maximum values.



Pulse Width Demodulation can be used to measure the input signal's high and low phases on the /INT2=J2 pin 19.

3.2.6 Power-save Mode

The B-Engine can be used for low power consumption applications. The power-save mode of the Am186ES reduces power consumption and heat dissipation, thereby extending battery life in portable systems. In power-save mode, operation of the CPU and internal peripherals continues at a slower clock frequency. When an interrupt occurs, it automatically returns to its normal operating frequency.

3.3 Am186ES PIO lines

The Am186ES has 32 pins available as user-programmable I/O lines. Each of these pins can be used as a user-programmable input or output signal, if the normal shared function is not needed. A PIO line can be configured to operate as an input or output with or without a weak pull-up or pull-down, or as an open-drain output. A pin's behavior, either pull-up or pull-down, is pre-determined and shown in the table below.

After power-on/reset, PIO pins default to various configurations. The initialization routine provided by TERN libraries reconfigures some of these pins as needed for specific on-board usage, as well. These configurations, as well as the processor-internal peripheral usage configurations, are listed below in Table 3.1.

PIO	*Function*	*Power-On/Reset status*	*B-Engine Pin No.*	*B-Engine Initial*
P0	Timer1 in	Input with pull-up	J2 pin 20	Input with pull-up
P1	Timer1 out	Input with pull-down	J2 pin 29	Input with pull-down
P2	/PCS6/A2	Input with pull-up	J2 pin 24	Input with pull-up
P3	/PCS5/A1	Input with pull-up	J2 pin 15	Input with pull-up
P4	DT/R	Normal	J2 pin 38	Input with pull-up Step 2
P5	/DEN/DS	Normal	J2 pin 30	Input with pull-up
P6	SRDY	Normal	J2 pin 35	Input with pull-down
P7	A17	Normal	U3 pin 22	A17
P8	A18	Normal	U3 pin 23	A18
P9	A19	Normal	J2 pin 10	A19
P10	Timer0 out	Input with pull-down	J2 pin 12	Input with pull-down
P11	Timer0 in	Input with pull-up	U7 EE pin 5	Input with pull-up
P12	DRQ0/INT5	Input with pull-up	U7 EE pin 6	Output for LED/EE/HWD
P13	DRQ1/INT6	Input with pull-up	J2 pin 11	Input with pull-up (USB)
P14	/MCS0	Input with pull-up	J2 pin 37	Input with pull-up (ET)
P15	/MCS1	Input with pull-up	J2 pin 23	Input with pull-up
P16	/PCS0	Input with pull-up	J1 pin 19	/PCS0
P17	/PCS1	Input with pull-up	U4 pin 4	HC138
P18	CTS1/PCS2	Input with pull-up	J2 pin 22	Input with pull-up
P19	RTS1/PCS3	Input with pull-up	J2 pin 31	Input with pull-up
P20	RTS0	Input with pull-up	J2 pin 27	Input with pull-up
P21	CTS0	Input with pull-up	J2 pin 36	Input with pull-up
P22	TxD0	Input with pull-up	J2 pin 34	TxD0
P23	RxD0	Input with pull-up	J2 pin 32	RxD0
P24	/MCS2	Input with pull-up	J2 pin 17	Input with pull-up
P25	/MCS3	Input with pull-up	J2 pin 18	Input with pull-up
P26	UZI	Input with pull-up	J2 pin 4	Input with pull-up*
P27	TxD1	Input with pull-up	J2 pin 28	TxD1
P28	RxD1	Input with pull-up	J2 pin 26	RxD1
P29	/CLKDIV2	Input with pull-up	J2 pin 3	Input with pull-up*
P30	INT4	Input with pull-up	J2 pin 33	Input with pull-up (ET)
P31	INT2	Input with pull-up	J2 pin 19	Input with pull-up

* Note: P26 and P29 must NOT be forced low during power-on or reset.

Table 3.1 I/O pin default configuration after power-on or reset

Three external interrupt lines are not shared with PIO pins:

INT0 = J2 pin 8
INT1 = J2 pin 6
INT3 = J2 pin 21

The 32 PIO lines, P0-P31, are configurable via two 16-bit registers, PIOMODE and PIODIRECTION. The settings are as follows:

MODE	PIOMODE reg.	PIODIRECTION reg.	PIN FUNCTION
0	0	0	Normal operation
1	0	1	INPUT with pull-up/pull-down
2	1	0	OUTPUT
3	1	1	INPUT without pull-up/pull-down

B-Engine initialization on PIO pins in **ae_init()** is listed below:

```
outport(0xff78,0xe73c);     // PDIR1, TxD0, RxD0, TxD1, RxD1, P16=PCS0, P17=PCS1
outport(0xff76,0x0000);     // PIOM1
outport(0xff72,0xec7b);     // PDIR0, P12,A19,A18,A17,P2=PCS6
outport(0xff70,0x1000);     // PIOM0, P12=LED
```

The C function in the library **ae_lib** can be used to initialize PIO pins.

void ***pio_init***(char bit, char mode);

Where bit = 0-31 and mode = 0-3, see the table above.

Example: ***pio_init***(12, 2); will set P12 as output

pio_init(1, 0); will set P1 as Timer1 output

void ***pio_wr***(char bit, char dat);

pio_wr(12,1); set P12 pin high, if P12 is in output mode

pio_wr(12,0); set P12 pin low, if P12 is in output mode

unsigned int ***pio_rd***(char port);

pio_rd (0); return 16-bit status of P0-P15, if corresponding pin is in input mode,

pio_rd (1); return 16-bit status of P16-P31, if corresponding pin is in input mode,

Some of the I/O lines are used by the B-Engine system for on-board components (Table 3.2). We suggest that you not use these lines unless you are sure that you are not interfering with the operation of such components (i.e., if the component is not installed).

You should also note that the external interrupt PIO pins INT2, 4, 5, and 6 are not available for use as output because of the inverters attached. The input values of these PIO interrupt lines will also be inverted for the same reason. As a result, calling ***pio_rd*** to read the value of P31 (**INT2**) will return 1 when pin 19 on header J2 is pulled low, with the result reversed if the pin is pulled high.

Signal	**Pin**	**Function**
P14	/MCS0	100M BaseT Ethernet
P4	/DT	STEP2 jumper
P11	Timer0 input	EE data input
P12	DRQ0/INT5	Output for LED or U7 serial EE clock or Hit watchdog
P17	/PCS1	HC138
P22	TxD0	Default SER0 debug
P23	RxD0	Default SER0 debug
/INT2	J2 pin 19	AD7606/7 busy
/INT4	J2 pin 33	Ethernet interrupt

Table 3.2 I/O lines used for on-board components

3.4 I/O Mapped Devices

3.4.1 I/O Space

External I/O devices can use I/O mapping for access. You can access such I/O devices with ***inportb***(port) or ***outportb***(port,dat). These functions will transfer one byte or word of data to the specified I/O address. The external I/O space is 64K, ranging from 0x0000 to 0xffff.

The default I/O access time is 15 wait states. You may use the function void ***io_wait***(char wait) to define the I/O wait states from 0 to 15. The system clock is 25 ns (or 50 ns), giving a clock speed of 40 MHz (or 20 MHz). Details regarding this can be found in the Software chapter, and in the Am186ES User's Manual. Slower components, such as most LCD interfaces, might find the maximum programmable wait state of 15 cycles still insufficient. Due to the high bus speed of the system, some components need to be attached to I/O pins directly.

For details regarding the chip select unit, please see Chapter 5 of the Am186ES User's Manual.

The table below shows more information about I/O mapping.

I/O space	Select	Usage
0x0100-0x011f	/AD	AD7606: U11 ADC
0x0120-0x013f	/DA	DA8544: U8 DAC
0x0140-0x015f	/CV	AD7606: U11 ADC
0x0160-0x017f	/RTC	72423: U10 RTC
0x0180-0x019f	LD	DA8544: U8 DAC
0x01a0-0x01bf	/L1	HC259: U5
0x01e0-0x01ff	/CF	Compact Flash: U11

3.5 Other Devices

A number of other devices are also available on the B-Engine. Some of these are optional, and might not be installed on the particular controller you are using. For a discussion regarding the software interface for these components, please see the Software chapter.

3.5.1 On-board Supervisor with Watchdog Timer

The MAX691/LTC691 (U6) is a supervisor chip. With it installed, the B-Engine has several functions: watchdog timer, battery backup, power-on-reset delay, power-supply monitoring, and power-failure warning. These will significantly improve system reliability.

Watchdog Timer

The watchdog timer is activated by setting a jumper on J5 of the B-Engine. The watchdog timer provides a means of verifying proper software execution. In the user's application program, calls to the function **hitwd()** (a routine that toggles the P12=HWD pin of the MAX691) should be arranged such that the HWD pin is accessed at least once every 1.6 seconds. If the J5 jumper is on and the HWD pin is not accessed within this time-out period, the watchdog timer pulls the WDO pin low, which asserts /RESET. This automatic assertion of /RESET may recover the application program if something is wrong. After the B-Engine is reset, the WDO remains low until a transition occurs at the WDI pin of the MAX691. When controllers are shipped from the factory the J5 jumper is off, which disables the watchdog timer.

The Am186ES has an internal watchdog timer. This is disabled by default with **ae_init()**.

Figure 3.1 Location of watchdog timer enable jumper

Battery Backup Protection

The backup battery protection protects data stored in the SRAM and RTC. The battery-switch-over circuit compares VCC to VBAT (+3 V lithium battery positive pin), and connects whichever is higher to the VRAM (power for SRAM and RTC). Thus, the SRAM and the real-time clock are backed up. In normal use, the lithium battery should last about 3-5 years without external power being supplied. When the external power is on, the battery-switch-over circuit will select the VCC to connect to the VRAM.

3.5.2 EEPROM

A serial EEPROM of 128 bytes (24C01), 512 bytes (24C04), or 2K bytes (24C16) can be installed in U7. The B-Engine uses the P12=SCL (serial clock) and P11=SDA (serial data) to interface with the EEPROM. The EEPROM can be used to store important data such as a node address, calibration coefficients, and configuration codes. It typically has 1,000,000 erase/write cycles. The data retention is more than 40 years. EEPROM can be read and written by simply calling the functions **ee_rd()** and **ee_wr()**. (Note: ee in these functions stands for EEPROM, not B-Engine)

The EEPROM uses the data input signal line, P11. A range of lower addresses in the EEPROM is reserved for TERN use. Details regarding which addresses are reserved, and for what purpose, can be found in Appendix B of this manual.

3.5.3 Real-time Clock RTC72423

If installed, the real-time clock RTC72423 (EPSON, U10) is mapped in the I/O address space 0x0600. It must be backed up with a lithium coin battery. The RTC is accessed via software drivers ***rtc_init()*** or ***rtc_rd()***.

It is also possible to configure the real-time clock to raise an output line attached to an external interrupt, at 1/64 second, 1 second, 1 minute, or 1 hour intervals. This can be used in a time-driven application, or the **VOFF** signal can be used to turn on/off the controller using an external switching power supply. An example of a program showing a similar application can be found in **`tern\186\samples\ae\poweroff.c`**.

3.5.4 AD7606 16-bit parallel and AD7607 14-bit high speed ADC

The BE supports either the AD7606, 16-bit ADC or the AD7607, 14-bit ADC. Both ADC's can accept ±10V or ±5V true bipolar analog signals while sampling at throughput rates up to 200 kSPS for all 8 analog inputs. Each analog input contains second-order antialansing filter, sample-and-hold amplifier and clamp protection tolerant up to ±16.5V. With 1M ohm analog input impedance, a 7000V ESD rating, and sustaining up to ±10 mA input current, the analog inputs are designed to survive in a rough industrial environment. The ***BE*** allows *simultaneous* sampling on all eight analog inputs. Using the 16-bit parallel DMA interface, the BE can transfer 8 channels of 16-bit (AD7606) or 14-bit (AD7607) data into the SRAM or CompactFlash with minimal software overhead.

See sample program \tern\186\samples\be\be_ad_ram.c and be_ad_cf.c for details on reading the ADC. The sample program is also included in the pre-built sample project: \tern\186\samples\be\be.ide.

3.5.5 DAC8544, 16-bit parallel high speed DAC

The DAC8544 is a low-power, quad-channel, 16-bit, voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail (0-5V) voltage swing to be achieved at the output.

A sample program **be_da.c** may be found in the **`c:\tern\186\samples\be`** directory.

3.5.6 100 MHz BaseT Ethernet

An WizNet™ Fast Ethernet Module can be installed to provide 100M Base-T network connectivity. This Ethernet module has a hardware LSI TCP/IP stack. It implements TCP/IP, UDP, ICMP and ARP in hardware, supporting internet protocol DLC and MAC. It has 16KB internal transmit and receiving buffer which is mapped into host processor's direct memory. The host can access the buffer via high speed DMA transfers. The hardware Ethernet module releases internet connectivity and protocol processing from the host processor. It supports 4 independent stack connections simultaneously at a 4Mbps protocol processing speed. An RJ45 8-pin connector is on-board for connecting to 10/100 Base-T Ethernet network. A software library is available for Ethernet connectivity.

3.5.7 Power Supply

The B-Engine must be powered by an external regulated 5V source. 5V DC power can be applied to J2.39=VCC and J2.40=GND, or J1.1=VCC and J1.2=GND. Many TERN expansion modules provide regulated 5VDC power. Below shows the BE with a VE232 that provices 5VDC as well as drivers for the RS232.

Figure 3.2 B-Engine with VE232

3.6 Headers and Connectors

3.6.1 Expansion Headers J1 and J2

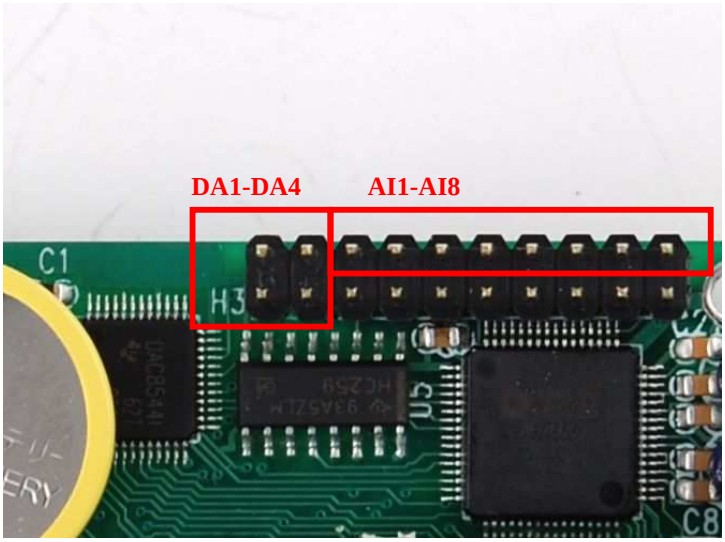
There are two 20x2 0.1 spacing headers for expansion. Most signals are directly routed to the Am186ES processor. These signals are 5V only, and any out-of-range voltages will most likely damage the board.

J2 Signal			
GND	40	39	VCC
P4	38	37	P14
/CTS0	36	35	P6
TXD0	34	33	/INT4
RXD0	32	31	/RTS1
P5	30	29	P1
TXD1	28	27	/RTS0
RXD1	26	25	
P2	24	23	P15
/CTS1	22	21	/INT3
P0	20	19	INT2
P25	18	17	P24
	16	15	P3
	14	13	
P10	12	11	P13
A19	10	9	
/INT0	8	7	/NMI
/INT1	6	5	
P26	4	3	P29
GND	2	1	

J1 Signal			
VCC	1	2	GND
	3	4	CLK
	5	6	GND
	7	8	D0
VOFF	9	10	D1
	11	12	D2
D15	13	14	D3
/RST	15	16	D4
RST	17	18	D5
P16	19	20	D6
D14	21	22	D7
D13	23	24	GND
	25	26	A7
D12	27	28	A6
/WR	29	30	A5
/RD	31	32	A4
D11	33	34	A3
D10	35	36	A2
D9	37	38	A1
D8	39	40	A0

3.6.2 H3 Connector for AD7606 and DAC8544

H3			
DA1	1	2	DA2
DA3	3	4	DA4
GND	5	6	AI8
GND	7	8	AI7
GND	9	10	AI6
GND	11	12	AI5
GND	13	14	AI4
GND	15	16	AI3
GND	17	18	AI2
GND	19	6	AI1



3.6.3 BE Header H3

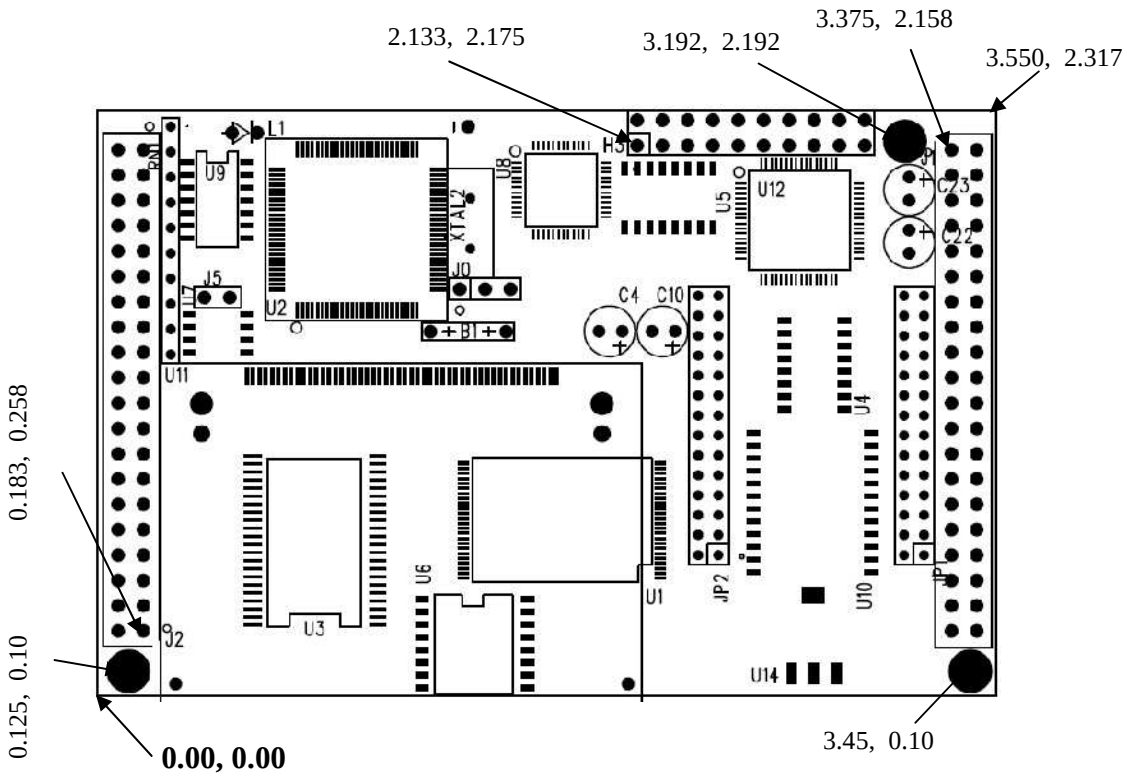
3.6.4 Jumpers

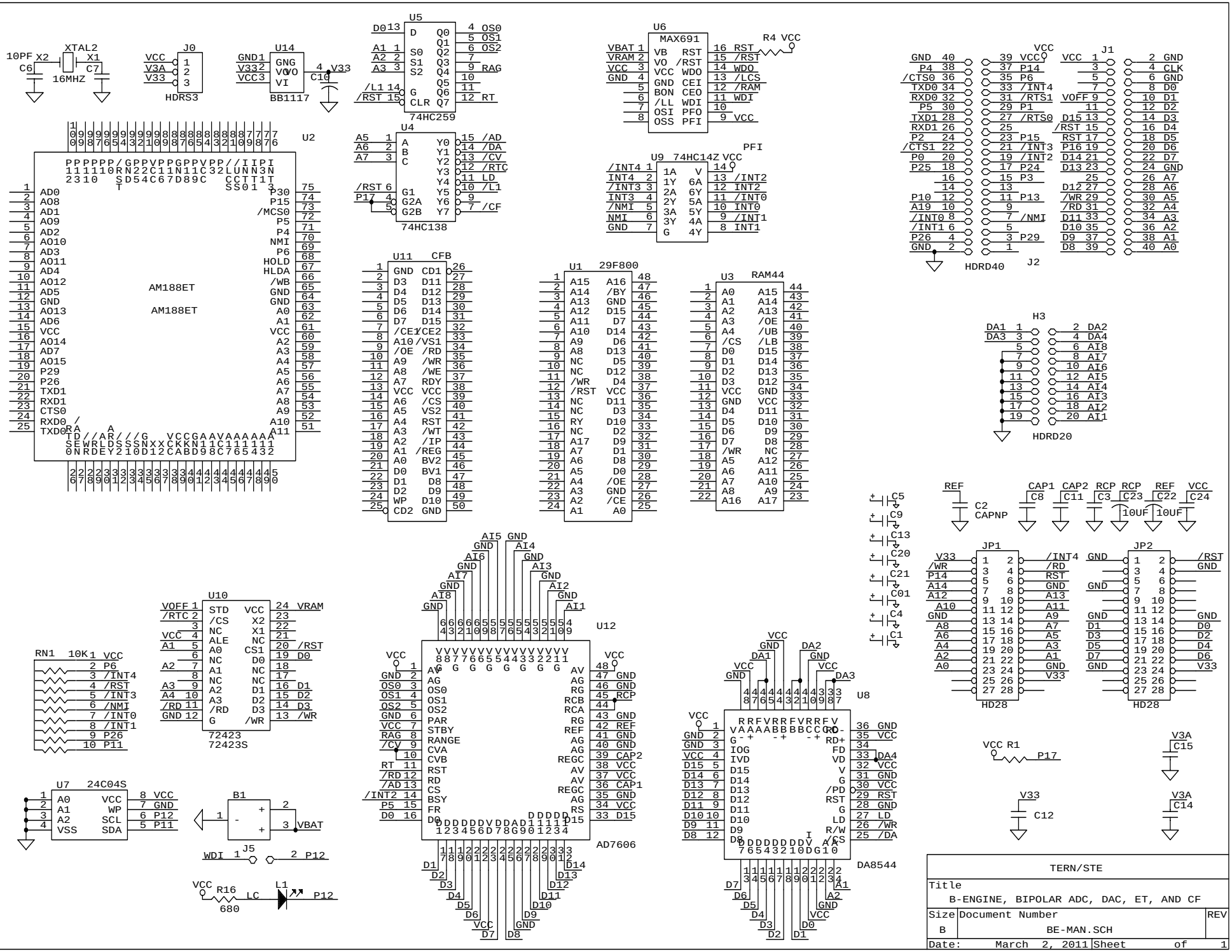
The following is a list of jumpers and connectors on B-Engine.

Name	Size	Function	Possible Configuration
J1	20x2	Main expansion port, A0-A7, D0-D15, /WR, /RD, P16,PFI,RST	
J2	20x2	Main expansion port, P*xx*, handshaking from SER2-9	Step 2 Jumper -> J2.38 = J2.40
J5	2x1	Watchdog timer	Enabled if Jumper is on Disabled if jumper is off

Appendix A: B-Engine Layout

All dimensions are in inches.




XTAL2
10PF X2 X1
C6 C7
16MHZ
J0
VCC 1
V3A 2
V33 3
HDRS3
U14
GND1 GNG
V332 VVO
VCC3 VI
BB1117
4 V33
C10
U5
D0 13
A1 1
A2 2
A3 3
/L1 14
/RST 15
D Q0
Q1
S0 Q2
S1 Q3
S2 Q4
Q5
G Q6
CLR Q7
4 OS0
5 OS1
6 OS2
7
9 RAG
10
11
12 RT
74HC259
U6
MAX691
VBAT 1
VRAM 2
VCC 3
GND 4
VB RST
VO /RST
VCC WDO
GND CEI
BON CEO
/LL WDI
OSI PFO
OSS PFI
16 RST
15 /RST
14 WDO
13 /LCS
12 /RAM
11 WDI
10
9 VCC
R4 VCC
U2
AM188ET
U4
A5 1
A6 2
A7 3
/RST 6
P17 4
5
A
B
C
G1
G2A
G2B
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
15 /AD
14 /DA
13 /CV
12 /RTC
11 LD
10 /L1
9
7 /CF
74HC138
U9 74HC14Z
/INT4 1
INT4 2
/INT3 3
INT3 4
/NMI 5
NMI 6
GND 7
1A 1Y
2A 2Y
3A 3Y
G
VCC 14
6A 13 /INT2
5A 12 INT2
4Y 11 /INT0
10 INT0
9 /INT1
8 INT1
PFI
J1
J2
HDRD40
U11 CFB
GND CD1
D3 D11
D4 D12
D5 D13
D6 D14
D7 D15
/CE1 CE2
A10 /VS1
/OE /RD
A9 /WR
A8 /WE
A7 RDY
VCC VCC
A6 /CS
A5 VS2
A4 RST
A3 /WT
A2 /IP
A1 /REG
A0 BV2
D0 BV1
D1 D8
D2 D9
WP D10
CD2 GND
U1 29F800
A15 A16
A14 /BY
A13 GND
A12 D15
A11 D7
A10 D14
A9 D6
A8 D13
NC D5
NC D12
/WR D4
/RST VCC
NC D11
NC D3
RY D10
NC D2
A17 D9
A7 D1
A6 D8
A5 D0
A4 /OE
A3 GND
A2 /CE
A1 A0
U3 RAM44
A0 A15
A1 A14
A2 A13
A3 /OE
A4 /UB
/CS /LB
D0 D15
D1 D14
D2 D13
D3 D12
VCC GND
GND VCC
D4 D11
D5 D10
D6 D9
D7 D8
/WR NC
A5 A12
A6 A11
A7 A10
A8 A9
A16 A17
H3
HDRD20
REF
C2
CAPNP
CAP1 C8
CAP2 C11
RCP C3
RCP C23
REF C22
VCC C24
10UF
10UF
C5
C9
C13
C20
C21
C01
C4
C1
JP1
JP2
HD28
HD28
U10
VOFF 1
/RTC 2
3
VCC 4
A1 5
6
A2 7
8
A3 9
A4 10
/RD 11
GND 12
STD VCC
/CS X2
NC X1
ALE NC
A0 CS1
NC D0
A1 NC
NC NC
A2 D1
A3 D2
/RD D3
G /WR
24 VRAM
23
22
21
20 /RST
19 D0
18
17
16 D1
15 D2
14 D3
13 /WR
72423
72423S
RN1 10K
1 VCC
2 P6
3 /INT4
4 /RST
5 /INT3
6 /NMI
7 /INT0
8 /INT1
9 P26
10 P11
U12
AD7606
U8
DA8544
U7 24C04S
A0 VCC
A1 WP
A2 SCL
VSS SDA
8 VCC
7 GND
6 P12
5 P11
B1
VBAT
J5
WDI 1
2 P12
VCC R16 LC L1 P12
680
VCC R1
P17
V3A C15
V33 C12
V3A C14
TERN/STE
Title
B-ENGINE, BIPOLAR ADC, DAC, ET, AND CF
Size B
Document Number
BE-MAN.SCH
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Date: March 2, 2011
Sheet of 1