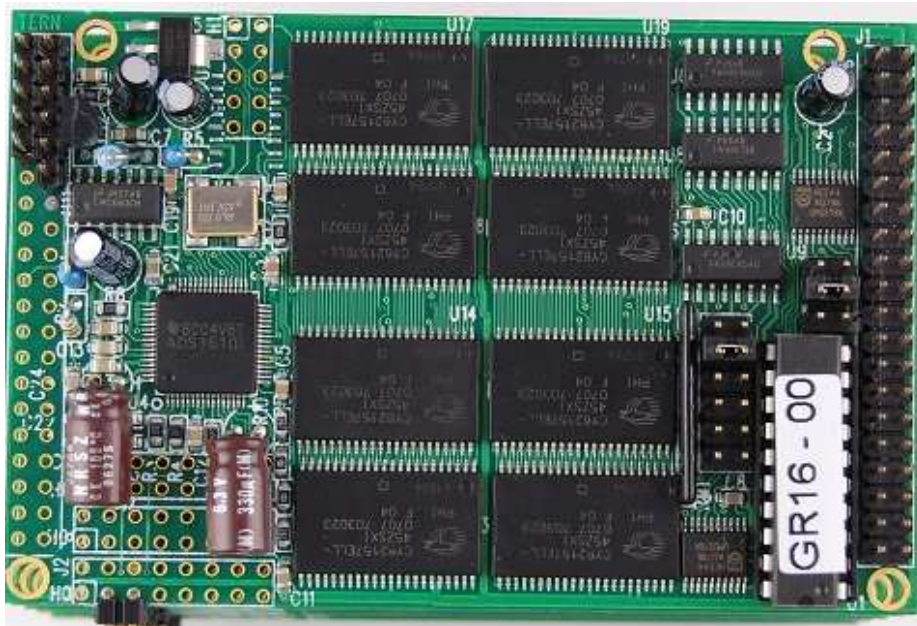


# *GR16*<sup>TM</sup>

*10 M SPS, 16-bit Analog Signal Digitizer  
up to 8MB FIFO*



## *Technical Manual*



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Version 2.00

October 7, 2010

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## 1.1 Functional Description

The GR16™ is an inexpensive high speed (up to 10M samples per second), 16-bit analog signal digitizer, designed to be driven by a host TERN 16-bit controller, such as 586-Engine, AE86, or EE.

The GR16™ supports a 16-bit Delta-Sigma ADC (ADS1610). With its outstanding high-speed performance, it is well-suited for demanding applications in data acquisition, scientific instruments, test equipment and communications.

The GR16™ is designed as an expansion board, measuring 2.3 by 3.6 inches, for TERN 16-bit controllers such as A-Engine86, 586-Drive, EE, and FN. The GR16™ interfaces to TERN host controller via 20x2 pins at J1, and 5x2 pins at J2.

## 1.2 ADS1610 16-Bit, 10 MSPS Analog-to-Digital Converter

The ADS1610 is a high-speed, high-precision, delta-sigma analog-to-digital converter (ADC) with 16-bit resolution. Inputs INP (H00.8) and INN (H00.6) are directly routed to the differential inputs of the ADS1610 without buffer circuits. The GR16™ also has two buffered inputs, A- (H0.3) and A+ (H0.5). A- and A+ are routed to INN and INP via 10 Ohm resistors. Analog input **signals** must be able to handle the load presented by the switching capacitors within ADS1610.

The GR16™ configures the ADS1610 with  $V_{REF} = 3V$  ( $V_{REFN} = 1V$  and  $V_{REFP} = 4V$ ). The 16-bit ADC data format is in binary two's complement. With  $V_{REFN} = 1V$  and  $V_{REFP} = 4V$ , the resulting input reference  $V_{REF} = (4V - 1V) = 3V$ . In this case, ADC outputs are:

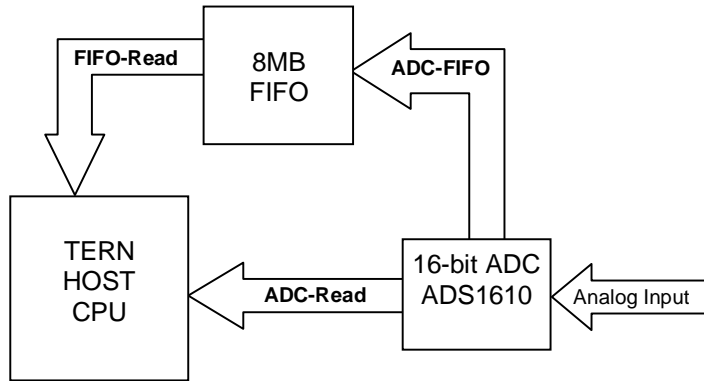
- When  $INP > INN$ , the ADC outputs 0-0x7FFF
- When  $INP < INN$ , the ADC outputs 0x8000-0xFFFF.
- When  $INP - INN = 3V$ , the ADC outputs 0x7FFF.
- When  $INN - INP = 3V$ , the ADC outputs 0x8000.
- When  $INN = INP$ , the ADC outputs 0 or 0xFFFF.

To achieve the highest analog performance, the recommended differential analog input voltage range is  $3V \times 0.891 = 2.67V$ . The absolute input voltage with respect to GND, on either INN or INP pin, must be within  $V_{REFN} = 1V$  to  $V_{REFP} = 4V$  range.

Recommended circuit designs are available when using single-ended or differential op amps, respectively. See ADS1610 data sheet for details ([www.ti.com](http://www.ti.com)). The GR16™ has an array of through-hole pads (H0, H00, H01) to allow installing user custom analog signal conditioning circuits.

### 1.3 ADC Sampling Modes

Three operation modes are available: **ADC-read**, **ADC-FIFO**, and **FIFO-read**. Figure 1.1 show the various sampling modes.



**Figure 1.1 ADC Sampling Modes**

In **ADC-read** mode, application software running on the host can read the 16-bit ADC data at any time. Sampling rate would be limited to CPU and application processing speed.

In **ADC-FIFO** mode, the GR16 can sample at far faster speeds (up to 10M samples per second). This data is recorded into the on-board FIFO SRAM. The ADC-FIFO operation is done entirely in hardware, without using any host CPU time.

Finally, the system can be set to **FIFO-read** mode. The host CPU can then read as much FIFO data as desired via I/O or DMA access.

### 1.4 ADC Sampling Frequency

The ADC sampling clock can be driven by on-board clock oscillator, as default, or an external clock. With a 60MHz on-board oscillator, the sample rate is 10M samples per second maximum. User can control the sampling rate by using an external clock, or selecting different dividers using onboard jumpers (H1). The default setting for H1 is H1.7 = H1.8 which is CLK/6 or 10MHz sample rate. In order to change the default setting, the trace on H1 must be cut before wiring a new jumper. Figure 1.2 shows the H1 header and default trace jumper on the back of the GR16™. Table 1.1 the various sample rates for each H1 setting.

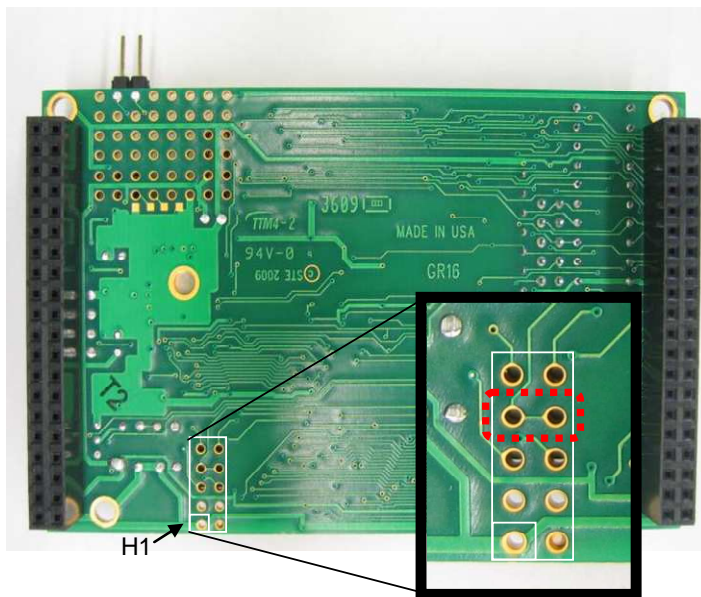


Figure 1.2 Frequency Divisor Jumper H1

Jumper Pins	Clock Divisor	Sample Rate for 60 MHz Oscillator
H1.8 (RDY) = H1.7 (CKI) * <b>DEFAULT</b> *	CLK / 6	10 MHz
H1.10 (CK1) = H1.7 (CKI)	CLK / 12	5 MHz
H1.9 (CK2) = H1.7 (CKI)	CLK / 24	2.5 MHz
H1.6 (CK3) = H1.7 (CKI)	CLK / 48	1.25 MHz
H1.5 (CK4) = H1.7 (CKI)	CLK / 96	625 kHz

Table 1.1 H1 Jumper Settings

## **1.5 ADC-FIFO Operation**

The **ADC-FIFO** operation runs when signals SA=0 and TR is active\*. The **ADC-FIFO** operation will stop immediately when SA=1. Setting AST low causes the FIFO counter to reset. When AST=1, SA=0 and TR is active\* the **GR16™** continues filling up the FIFO with ADC readings until the selected recording length is reached forcing SA high (SA=1). The record length of the FIFO can be configured via jumper block H3. Available data lengths include 8MB (H3.4 = H3.3), 4MB (H3.4 = H3.2), or 512KB (H3.4 = H3.6).

The hardware trigger signal (TR) is routed to header locations H2.7 and H1.2. By default H2.7 and H2.8 are jumpered (H2.7=H2.8=GND) forcing TR=0\*. It is important that the external hardware trigger signal (TR) must stay active while the **GR16™** is recording ADC readings.

The FIFO will retain recorded data until it's powered-off or a new **ADC-FIFO** operation is initiated. To read data from the FIFO, reset the counter by bringing AST low then high, then read from the FIFO. Every **FIFO-read** increments FIFO address.

## **1.6 GR16™ Stacks**

Multiple **GR16™** units can be stacked via pass through sockets on J1 and J2. H2 pin 10=/PCS is the host I/O chip select. While H2.10=H2.9, as default, the Host controller J1.19 is the base I/O chip select. For each /PCS setting, there are 4 GAL chips available: GRAB1600, GRAB1640, GRAB1680, and GRAB16C0. Base I/O address are 0x00, 0x40, 0x80, and 0xC0 for these 4 GALs.

Stacked **GR16™** units can share a common external CK and SYNC signal on H1 header. With the CK inputs running, pulse the common shared SYNC line for the units to synchronize simultaneous conversions. Be aware that CK and SYNC signals are directly routed to ADS1610, with a voltage range of 0V-3.3V. Over voltage will damage ADS1610 ADC.

## **1.7 GR16-LM™ Version**

GR16-LM version uses a different GAL set (GR16-00, GR16-40, GR16-80, and GR16-C0) that have an active high trigger TR. This version operates when TR=1. By using an active high trigger, the SA output from one GR16 can trigger the TR signal of another GR16 allowing uninterrupted analog acquisition between GR16s. By default, H2.7 (TR) is not jumpered to GND at H2.8 on the GR16-LM version.

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\*The original version of GR16 uses an active low (TR=0) trigger. The GR16-LM version uses a different GAL that has an active high trigger. This version operates when TR=1. GR16-LM versions can be identified by the GAL labels: GR16-00, GR16-40, GR16-80, and GR16-C0.

## 1.8 GR16 Photos

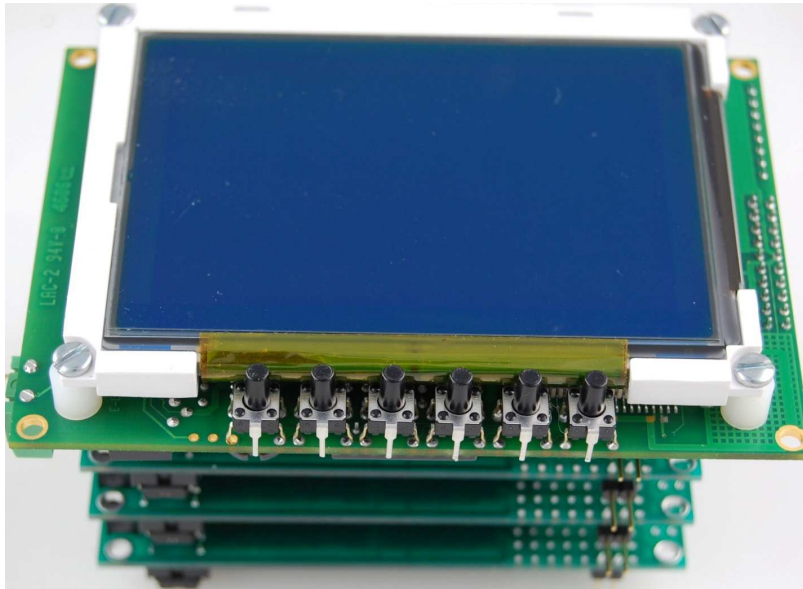


Figure 1.3 Front view of an EL controller with 4 GR16s.

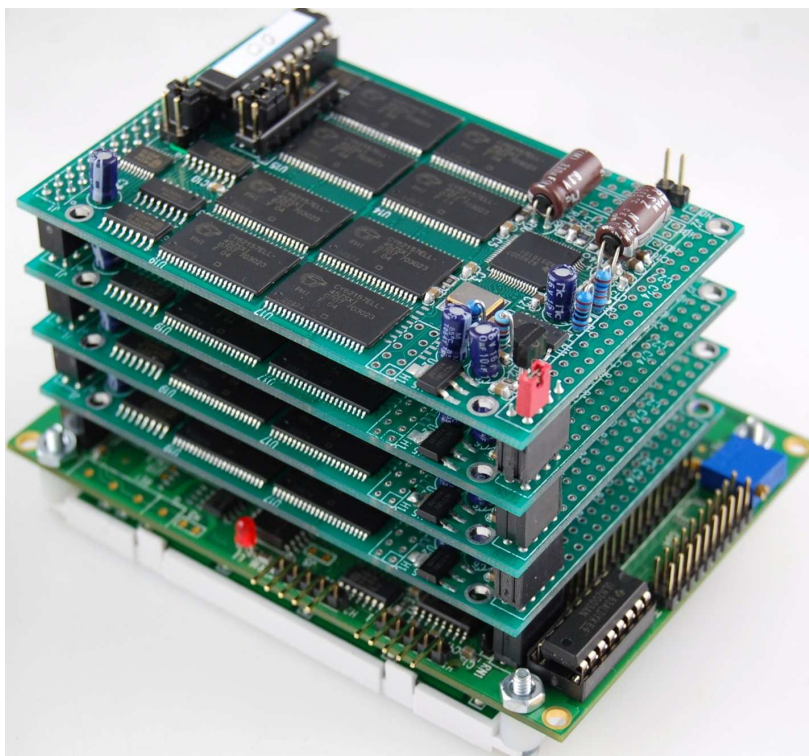


Figure 1.4 Back view of an EL controller with 4 GR16s.

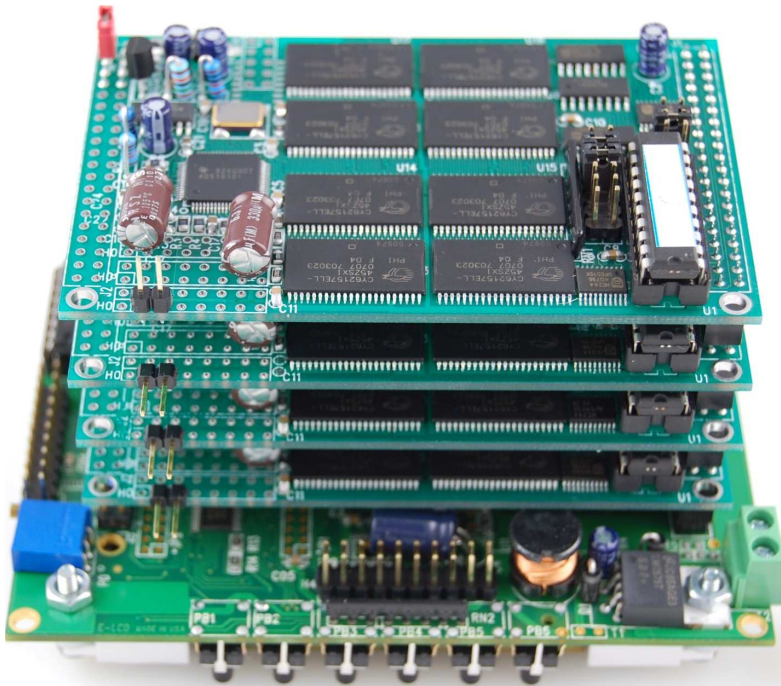


Figure 1.5 Side view of a EL controller with 4 GR16s.

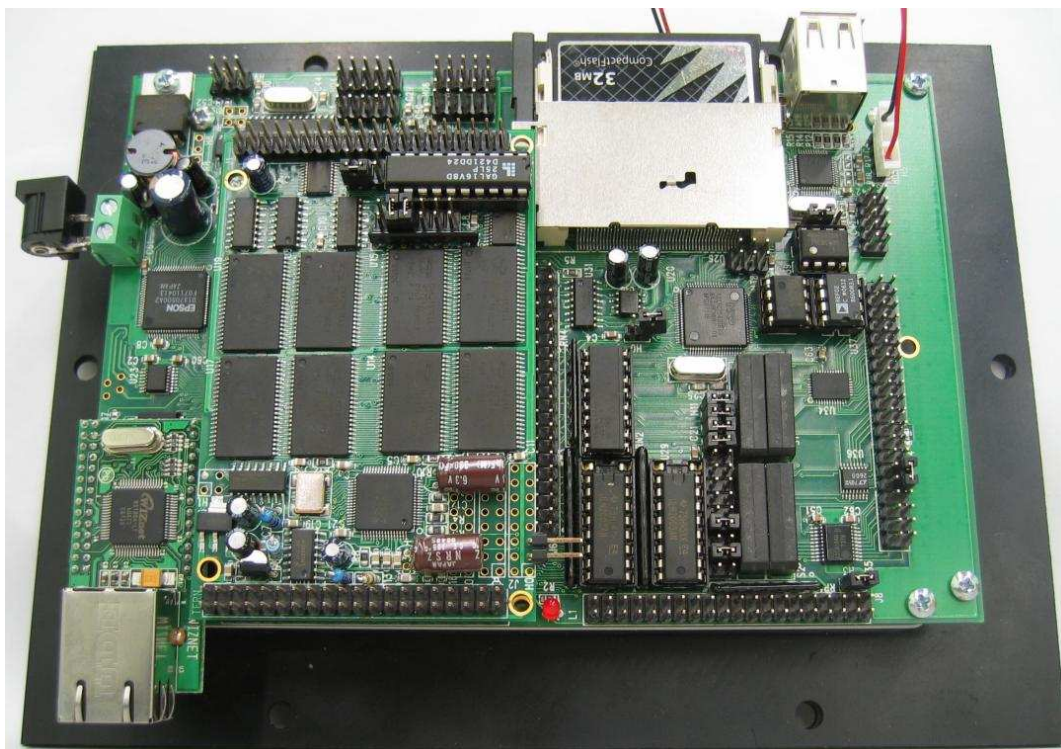


Figure 1.6 UD with GR16™



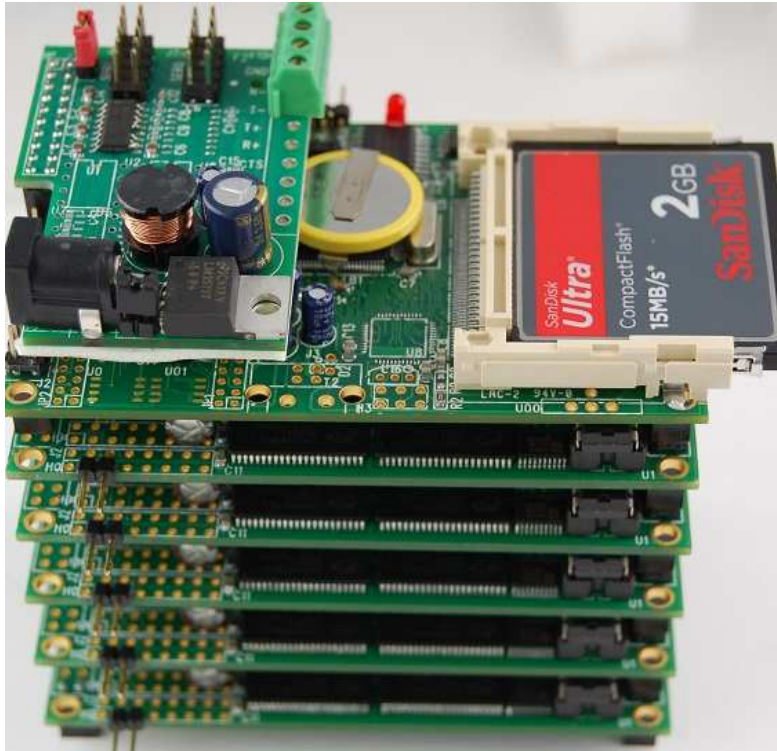


Figure 1.7 E-Engine with VE232 stacked on five GR16s powered by 9-30V



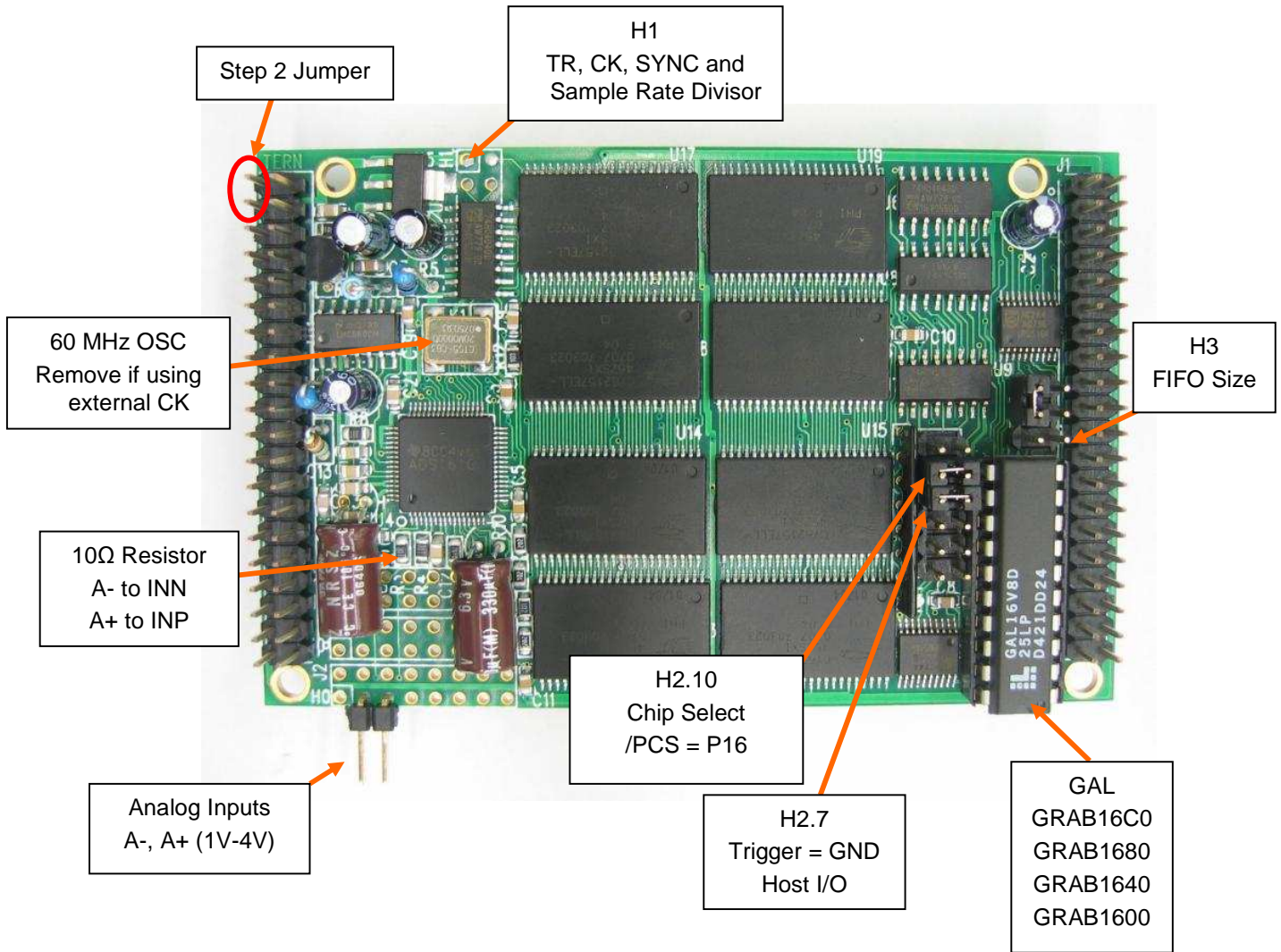
Figure 1.8 E-Engine with stacked on five GR16s powered by external 5V

## **1.9 Features**

- 2.3 x 3.6 x 0.5 inches
- 200 mA at 5V DC power per GR16
- High-Speed Delta-Sigma ADC (ADS1610)
- User Programmable Sample Rate, up to 10M SPS
- On-Chip Digital Filter Simplifies Anti-Alias
- User configurable FIFO data size, up to 8MB.
- Stackable multi units sharing Sync, and Trigger.
- On-board oscillator or external host clock.
- Driven by a 16-bit TERN controller
- Support ADC read, ADC-FIFO, FIFO-read modes
- Software programmable Power off mode controlled by PD signal.

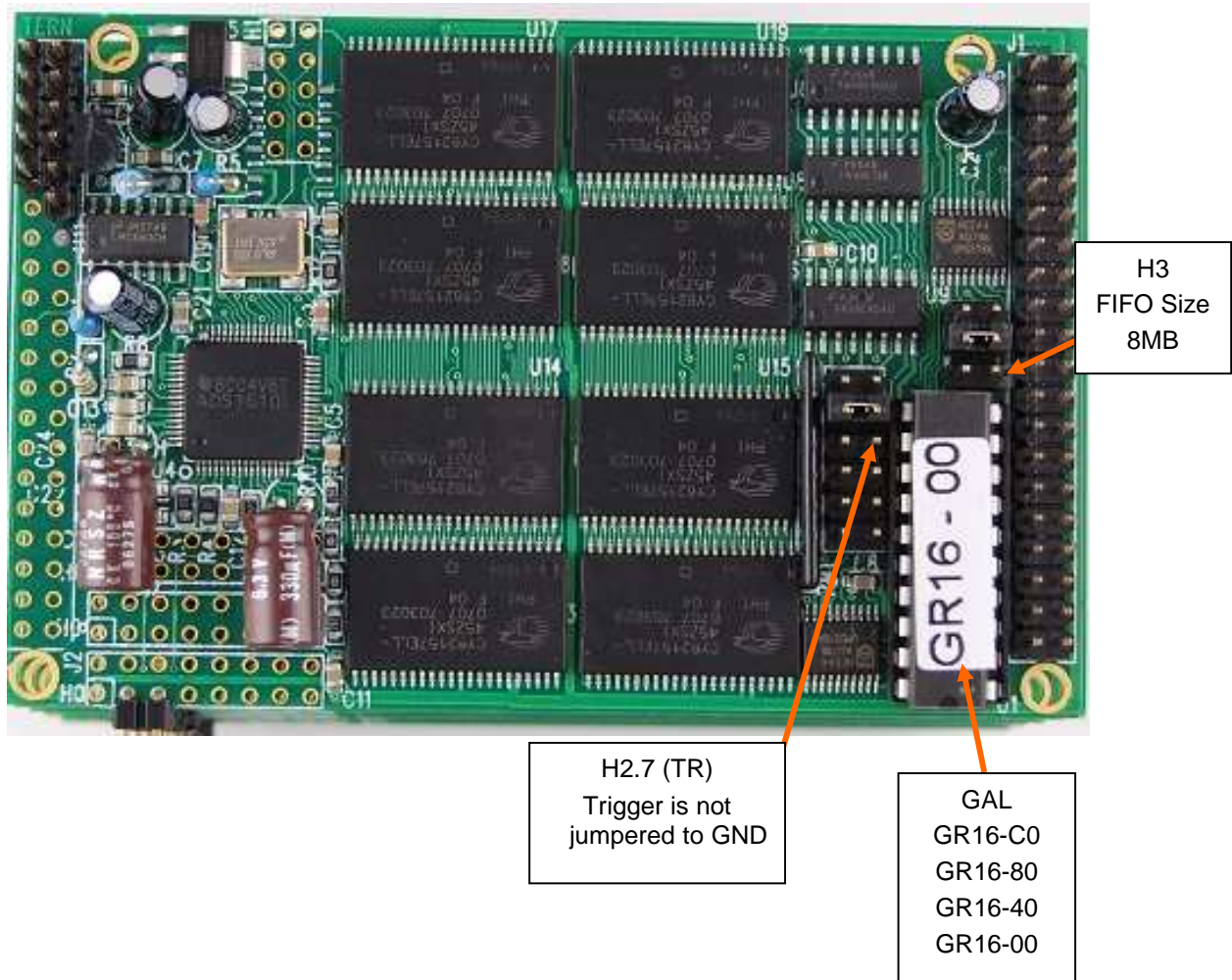
### 1.10 GR16 Physical Description

The figure below shows the physical layout of the GR16 board.



### 1.11 GR16-LM Physical Description

The GR16-LM version is the same hardware as the regular GR16, but uses a different GAL set. The jumpers are set differently to accommodate the active high trigger TR.



## 1.12 GR16 Fifth Board Physical Description

When stacking more than four GR16s, a different chip select must be used to operate boards 5 through 8. The image below shows the jumper setting for the 5<sup>th</sup> GR16.

