Grabber™

80 MHZ Analog Signal Digitizer

Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Functional Description

The ***Grabber™*** (**GR**) is a high speed, analog signal digitizer board.

Features:

- 2.3 x 3.6 x 0.5 inches
- 80 MHz, 8-bit ADC, with front signal conditioning
- 5V DC only, driven by AE/AE86/BBA/SL/A104//IE/IEM/IEP/ID
- 2 KB 10 ns FIFO for 80MHz ADC data
- Two channels of 10 MHz ADC with two 512KB SRAMs for data storage
- Clock selectable from on-board oscillator, external, or host controller clock.
- Trigger window based on “one shot”, from an external pulse or host controller I/O.
- Analog input signal conditioning with front amplifier.

The **GR** supports two channels of high speed analog signal digitizers. Each channel consists an 8-bit 40/80 MHz ADC (AD9057, Analog Devices), an 160 MHz Rail-to-Rail front amplifier (AD8041, Analog Devices), and a 512KB SRAM FIFO.

An optional high speed 2KB FIFO (IDT72231, or CY7C4231) can be installed to store ADC data up to 80 MHz.

Two ADC channels are driven by the same clock and same address generator, so two analog signals can be digitized and recorded simultaneously. The ADC clock can be selected, via H1 header, from an on-board clock oscillator, or host controller’s clock, or an external clock.

The ADC can operate continuously at full clock speed, but the ADC data can only be stored in the FIFO within a trigger window, while /WRFF low active. A trigger signal can be generated by a host controller’s I/O pin (P14 for example), or by an external trigger pulse with a 74HC221 “one shot”. The conversion and the recording can not be stopped until the pre-select address size reached. A address generator can be reset by software, or reset by reaching a pre-set address. There are 3 length of ADC data can be selected via H2 jumper: 32KB, 128KB, or 512KB. When the address reaches the selected length, the ADC conversion stopped, and the address generator reset to zero, ready for the host controller to read out ADC data. The ADC data can only be read in the sequence of “First In First Out”. Only one channel ADC data can be read out continuously at a time. Each read operation by the host controller will increment the address.

The host controller can also directly read each ADC without store any data in the FIFO RAM. It will be useful during a calibration.

The ***GR*** is designed as an expansion board, measuring 2.3 by 3.6 inches, for TERN controllers such as A-Engine/i386-Engine/BB-A. The ***GR*** interface to the host controller via 20x2 pins at J1, and 10x2 pins at J2.

By default, the valid analog signal input voltage level at J4, and J5 header should be 1V peak to peak, and centered at 2.5V. So the valid analog input signal should be in the voltage range of 2V to 3V.

I/O Map

All devices on the **GR** are I/O mapping for host controller access. You can access such I/O devices, using J1 pin 19 /PCS0, with ***inportb***(port) or ***outportb***(port,dat). These functions will transfer one byte or word of data to the specified I/O address.

The table below shows more information about I/O mapping.

I/O space	Select	Usage	Location
0x0080	/PCS0	Reads address status, SA	H2 pin 4
0x0090	/PCS0	Reads Write window status, /WRFF	H2 pin 12=/WRFF
0x00b0	/PCS0	Write D0 to PWD. Low=ADC active	U4 pin 1
0x00a0	/PCS0	Write D0 to /RESET. High=reset address	U6 pin 11
0x00c0	/PCS0	Read U4 ADC, if PWD=0	
0x00c0	/PCS0	Read U7 RAM, if PWD=1	
0x00d0	/PCS0	Read U04 ADC, if PWD=0	
0x00d0	/PCS0	Read U07 RAM, if PWD=1	

Usage of Controller I/O Pins

P14=J2 pin 37. Start digitizing if P14 high via Jumper H2 pin 10 (P14)=pin12 (/WRFF).

/CTS1=J2 pin 22, /PCS0=J1 pin 19, /RTS1=J2 pin 31 are used for optional base peripheral chip select via H1 header to pin 4=/PCS.

/INT4=J2 pin 33, may use as input or interrupt for U5 FIFO pin 14, and H2 pin 7.

J1 pin 4 = CLK1=H1 pin 9.

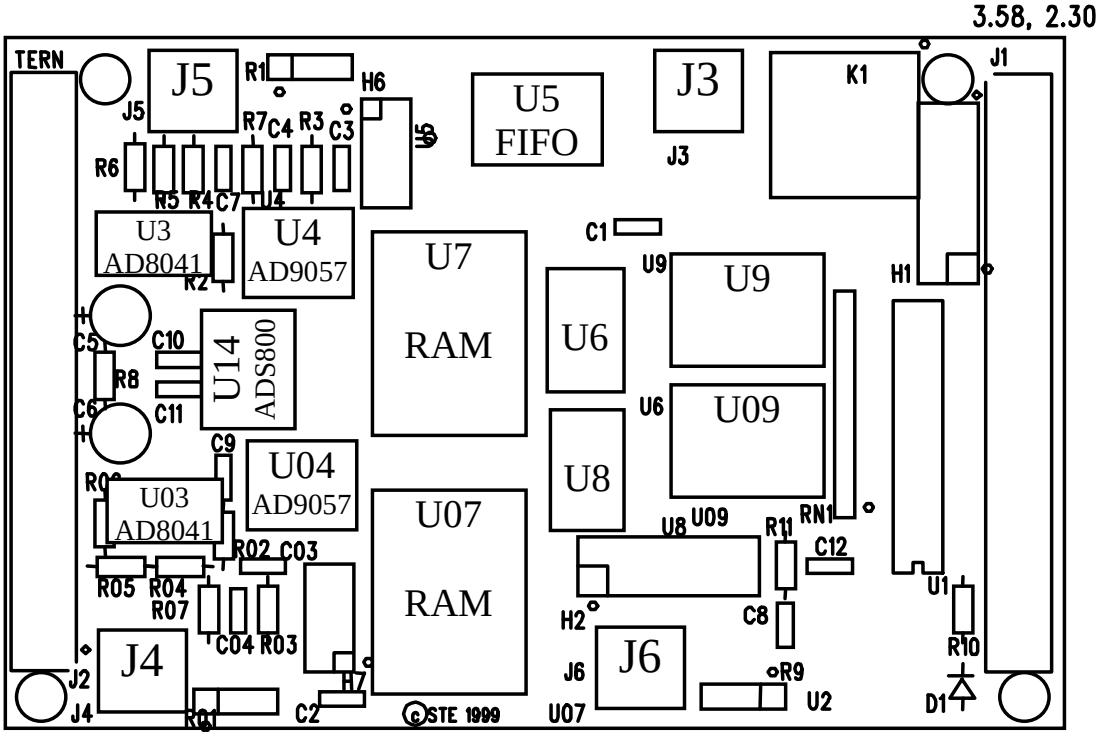
For A-Engine, J1 pin 4=P1 (Timer1 output).

For A-Engine86, J1 pin 4 = 40 MHz system CLK. It is too fast to use. User may use J2 pin 29=P1 as digitize clock, or use external clock, or install a oscillator in K1.

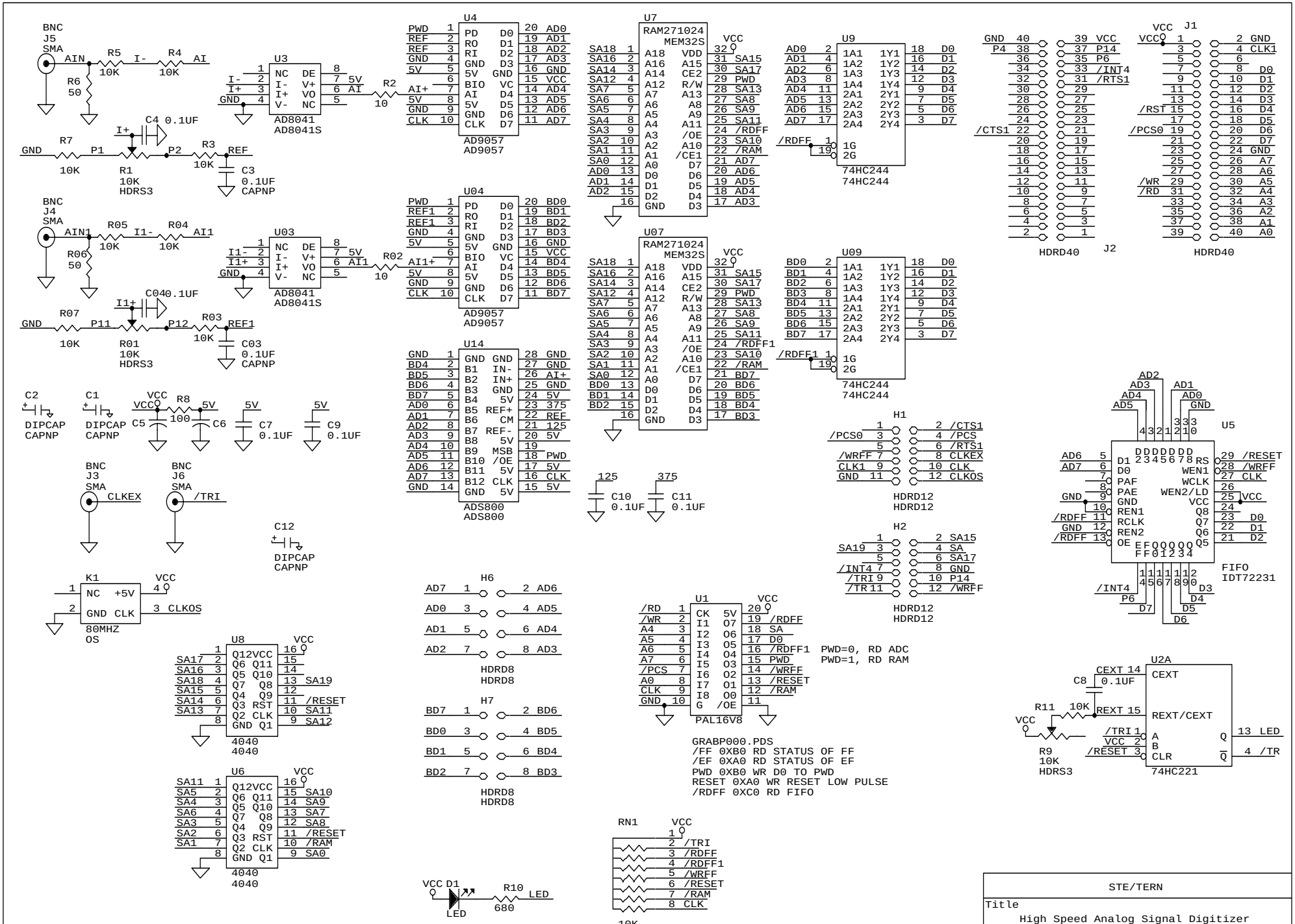
Optional SMA connectors can be installed on J3, J4, J5, and J6, replacing pin headers.

Please read the grabber schematic included in the CD for more details.

A sample program grabber.c is available.



Grabber Layout, ***Mar. 1, 2000***


BNC J5 SMA AIN R5 10K I- R4 10K AI R6 50
U3 AD8041 AD8041S R2 10 AI+ I- I+ GND 5V
U4 AD9057 AD9057
C4 0.1UF I+ R7 10K GND P1 P2 R3 10K REF R1 10K HDRS3 C3 0.1UF CAPNP
BNC J4 SMA AIN1 R05 10K I1- R04 10K AI1 R06 50
U03 AD8041 AD8041S R02 10 AI1+ I1- I1+ GND 5V
U04 AD9057 AD9057
C040.1UF I1+ R07 10K GND P11 P12 R03 10K REF1 R01 10K HDRS3 C03 0.1UF CAPNP
U7 RAM271024 MEM32S U07 RAM271024 MEM32S VCC
U9 74HC244 74HC244 U09 74HC244 74HC244 /RDFF /RDFF1
J2 HDRD40 J1 HDRD40
C2 DIPCAP CAPNP C1 DIPCAP CAPNP VCC R8 100 5V C5 C6 C7 0.1UF C9 0.1UF
U14 ADS800 ADS800
C10 0.1UF C11 0.1UF 125 375
H1 HDRD12 HDRD12 H2 HDRD12 HDRD12
U5 FIFO IDT72231
BNC J3 SMA CLKEX BNC J6 SMA /TRI
C12 DIPCAP CAPNP
K1 80MHZ OS
U8 4040 4040 U6 4040 4040
H6 HDRD8 HDRD8 H7 HDRD8 HDRD8
U1 PAL16V8
PWD=0, RD ADC
PWD=1, RD RAM
GRABP000.PDS
/FF 0XB0 RD STATUS OF FF
/EF 0XA0 RD STATUS OF EF
PWD 0XB0 WR D0 TO PWD
RESET 0XA0 WR RESET LOW PULSE
/RDFF 0XC0 RD FIFO
U2A 74HC221 C8 0.1UF R11 10K CEXT REXT VCC /TRI /RESET R9 10K HDRS3
VCC D1 LED R10 680 LED
RN1 10K RN8S1
STE/TERN
Title
High Speed Analog Signal Digitizer
Size B
Document Number grab.SCH
REV
Date: November 26, 1999
Sheet 1 of 1