MemCard-A™

Low-cost 68-pin PCMCIA ATA Flash Memory Card interface
for TERN controllers
Supports up to 420 MB, ADC, Ethernet

Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

The MemCard-A (MM-A) is a multifunctional I/O expansion board for TERN controllers. The MM-A supports a 68-pin PCMCIA socket for ATA-type flash memory cards. You may also install up to six channels of 24-bit ADC (LTC2400) and up to 33 channels of 12-bit ADC (TLC2543). A 10Base-T Ethernet interface based on the CS8900 (Crystal Semiconductor Corporation) ethernet controller can also be installed. The MM-A can be installed on many of TERN's controllers, such as the A104, A-Engine, A-Engine-P, BirdBox-A, i386-Engine, i386-Engine-P, SmartLCD, or V25-Engine via a 20x2 pin header.

Measuring only 3.6 x 2.3 x 1.2 inches, the MM-A can be added onto TERN controllers to provide additional memory and other features. It supports up to 420 MB additional mass data storage, up to 39 channels of analog signal inputs, and an ethernet interface. It can be used as a general I/O expansion solution for many portable embedded applications.

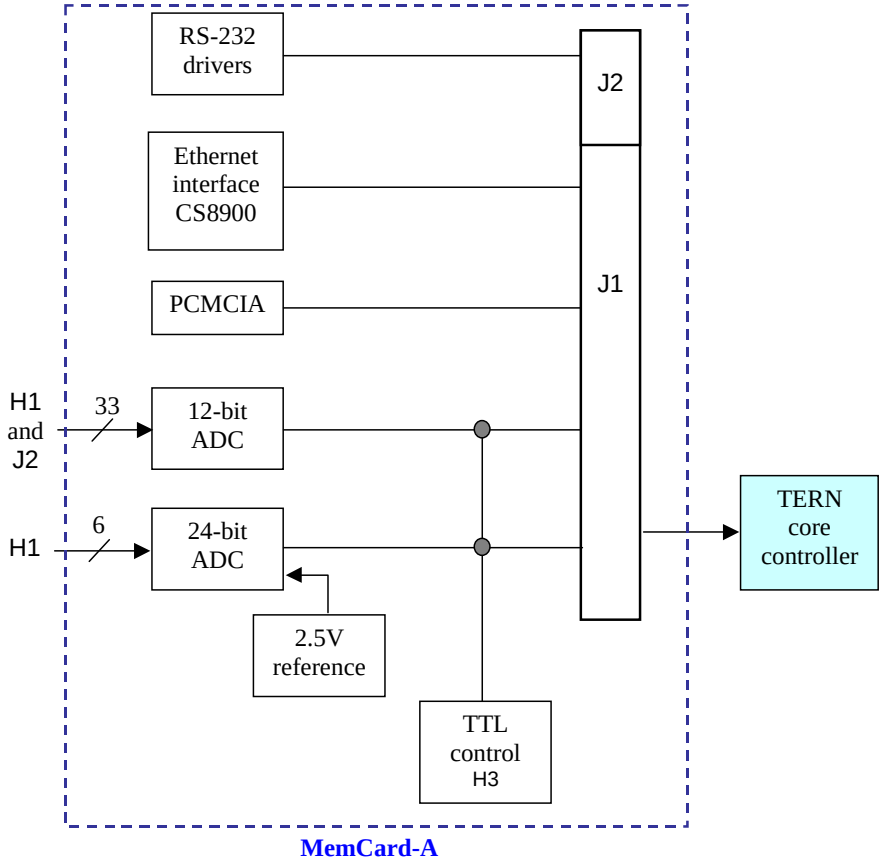


Figure 1.1 Functional block diagram of the MemCard-A

Two channels of RS-232 drivers and a 5V linear power regulator can be installed to support TERN's Engine-type controllers.

The ADC analog circuits of the MM-A can also be driven with five TTL outputs and two input signals at H3. Any other controller or application that needs 24-bit ADC or 12-bit ADC inputs can interface to the MM-A with I/O pins.

PCMCIA Interface

With a 68-pin PCMCIA/JEIDA international standard memory card interface, the MM-A supports ATA Flash memory cards. ATA cards provide high-capacity, solid-state flash memory that electrically compiles with the Personal Computer Memory Card International Association ATA standard. Several vendors, such as SanDisk, M-Systems, and Simple Technology, supply ATA cards. The ATA card includes an on-card intelligent controller that provides a high-level interface to the host controller. This interface allows TERN controllers to use the MM-A to interface to various sizes of ATA cards via the same hardware and software interface. TERN controllers can issue the standard sets of ATA software commands to the ATA card to read or write blocks of memory. A block of memory (a sector) consists of 512 bytes of data and is protected by a powerful Error Correcting Code (ECC).

The ATA card can only be read or written to one sector (512 bytes) at a time. The time required to write to one sector is 3.76 ms, or approximately 7.3 μs per byte. The ATA card will be busy for 9 ms before you can write the next 512 bytes. You may collect 512 bytes of ADC data in the SRAM first, and then write data into PCMCIA when the ATA card is not busy. See the sample programs **mma_time.c** and **mm_disk.c** in the **`c:\tern\186\samples\mma`** directory.

The ATA card's on-card intelligent controller manages interface protocols, data storage, and retrieval, as well as ECC, defect handling and diagnostics, power management, and clock control. It simplifies the interface to the host controller in terms of hardware and software. TERN's EV/DV Kit has software library drivers and sample programs for users to easily write or read the ATA card. You have to read or write at least one sector, or 512 bytes, at once.

Ethernet

The Ethernet LAN Controller on the MM-A is the CS8900 from Crystal Semiconductor Corporation (512-445-7222). The CS8900 includes on-chip RAM and 10BASE-T transmit and receive filters. The CS8900 directly interfaces to the TERN controller's data bus, providing a high-speed, full duplex operation. The MM-A interface to the Ethernet is via a standard RJ45 8-pin connector. The CS8900 offers a broad range of performance features and configuration options. Its unique PacketPage architecture automatically adapts to changing network traffic patterns and available system resources. The CS8900-based MM-A can increase system efficiency and minimize CPU overhead in a 10BASE-T network. The MM-A with CS8900 provides a true full-duplex Ethernet solution, incorporating all of the analog and digital circuitry needed for a complete C/C++ programmable Ethernet node controller.

24-bit ADC

Up to six 24-bit ADC surface-mount chips (LTC2400, Linear Technology) can be installed on the MMA. The LTC2400 is a 24-bit analog-to-digital converter with an integrated oscillator. It uses delta-sigma technology, providing a typical conversion time of 160 ms. Based on the LTC2400 data sheets, it can provide 24-bit ADC data, with 4 ppm full-scale error with no missing codes.

A 3-pin header (H4) is installed on the MM-A to configure the LTC2400 for better than 110 dB noise rejection at 50 Hz (H4 1-2) or at 60 Hz (H4 2-3). The 24-bit ADC uses an on-board external reference of 2.5V. Each ADC communicates with a 3-wire digital interface. Three TTL lines are required to drive a LTC2400: SCK (clock to the chip), /CS (chip select=L0-L5), and D24 (24-bit serial data output from the chip). If the chip select line (L0-L5) is high, the TLC2400 is disabled, and D24 line is in high-impedance state.

12-bit ADC

Up to three 12-bit ADC surface-mount chips (TLC2543, TI) can be installed on the MMA. The TLC2543 is a 12-bit, switched-capacitor, successive-approximation, 11 channels, serial interface, analog-to-digital

converter. Four TTL I/O lines are required to handle the ADC: /CS (chip select=L0, L1, or L2)); SCK (clock to the chip); DIN (serial command data to the chip); and D12 (12-bit serial data output from the chip). If chip select line is low, the TLC2543 will have output on D12. If the chip select line is high, the TLC2543 is disabled and D12 is in high-impedance state. The serial access allows a conversion rate of up to approximately 10 KHz for a 40 MHz A-Engine.

A reference voltage of VCC (+5V) can be provided to the 12-bit ADC **REF+** via the 3-pin header H2 pin 1-2. The on-board precision 2.5V reference can be connected to the **REF+** pin via H2 pin 2-3.

The CLK signal to the ADC is toggled through an I/O pin, and the serial access allows a conversion rate of up to approximately 10 KHz.

Analog signal inputs are routed at the J2 and H1 headers. A total of 22 channels of 12-bit ADC inputs, AD10 to AD2a, are routed to J2. Six channels of 24-bit ADC inputs (V1 to V6) and 11 channels 12-bit ADC inputs AD30 to AD3a are routed to the 10x2 pin header H1.

74HC259

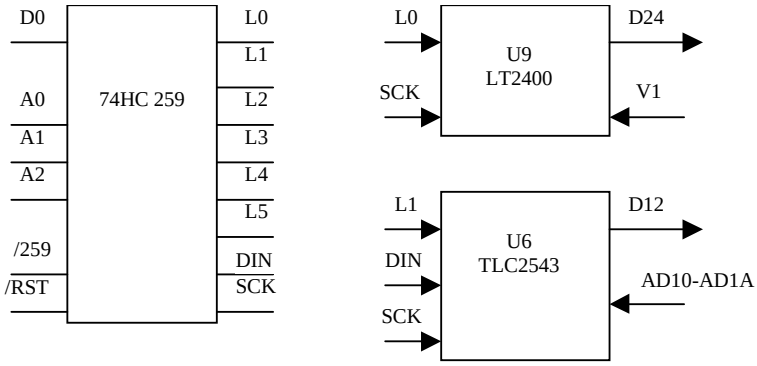


Figure 1.2 Functional block diagram for 74HC259 and ADCs

In order to generate the necessary TTL control signals for the 12-bit and 24-bit ADCs, an 8-bit addressable data latch (74HC259) is on-board. It is capable of storing single-line data (D0) in eight addressable (A0-A2) latches (L0-L5, DIN, SCK). There are three address lines, A0-A2, to select the D0 to Lx latched output. The D0 line is the data line to be latched into one of the eight TTL outputs L0-7 (L6=DIN, L7=SCK). A low active chip select line (/259) should be remain high while address and data lines are changing, and it will latch the D0 into the output pin selected by the A0-A2 while /259 change to low, then to high. Of the eight TTL outputs, L6=DIN and L7=SCK are used for ADC serial clock and data input. The other six TTL outputs, L0 to L5, can be used to select 12-bit or 24-bit ADCs. Please refer to the attached schematics for more details.

Sample programs for using the A-Engine to drive ADCs can be found in **`c:\tern\186\samples\mma\mma_ad24.c`**, and a sample program to demo using V104 I/O pins to drive ADCs can be found in **`c:\tern\v25\v104\v104ad24.c`**.

LT1019

The MM-A uses an LT1019-2.5 (3ppm/°C) as a precision reference voltage. The LT1019 has a typical ultra-low temperature drift of 3ppm/°C. It can sink and source up to 10 mA. The LT1019 has a TEMP pin. The voltage on this pin is directly proportional to absolute temperature (PTAT) with a slope of approximately 2.1 mV/°C. Room temperature (295°K) voltage is therefore approximately 2.1 x 295°K = 620 mV. The TEMP pin can be used to sense chip or board temperature in applications where the LT1019 is forced to sense ambient temperature. Typical chip temperature rise over ambient is 2°C. In applications

that use thermocouples, TEMP could be used to sense the connector block temperature, if the temperature difference between block and chip is tolerable or can be calibrated out. The temperature difference between the block and chip may be reduced by a thermoconductive contact. The TEMP voltage is connected to H1 pin 13.

Power Input

You may power the MM-A with +9V to +12V unregulated DC on the 2-pin header H5 with a linear regulator LM7805 installed in U18. You may power the MM-A with regulated 5V at J2 pin 39, if you are not using the on-board linear regulator.

You can install the MM-A directly on a TERN core controller, such as the A-Engine, via the 20x2 pin J1 header. The MM-A can also be used with other TERN controllers such as the V104 by connecting it with a cable via TTL pins.

1.2 Features

- Dimensions: 3.58 x 2.30 x 0.70 inches
- Power supply input voltage range:
  +8V to +12V with regulator
- or, regulated 5V without the regulator installed
- 68-pin PCMCIA card interface, supports ATA-type PC Flash memory cards up to 240 MB from SanDisk, M-Systems, and Simple Technology*
- Up to 6 channels of 24-bit ADC*
- On-board 3 ppm/degree C precision 2.5V reference and on-board temperature sensor*
- Up to 33 channels of 12-bit ADC, 0 to 5V input*
- Two channels of RS-232 serial drivers*
- 10 BASE-T Ethernet interface includes CS8900 controller, RJ45, transformer, and filter*
- Easy to install directly on a TERN core controller
  (A104, A-Engine, A-Engine-P, BirdBox-A, i386-Engine, IE-P, SmartLCD, or V25-Engine)
- Easy to connect with a cable to any other TERN controllers (V104, etc.) via TTL pins

  * available as an option

1.3 Physical Description

Figure 1.3 shows the physical layout of the MemCard-A. The MemCard-A is used as an expansion board for the TERN core controllers such as the A-Engine, SmartLCD, etc.

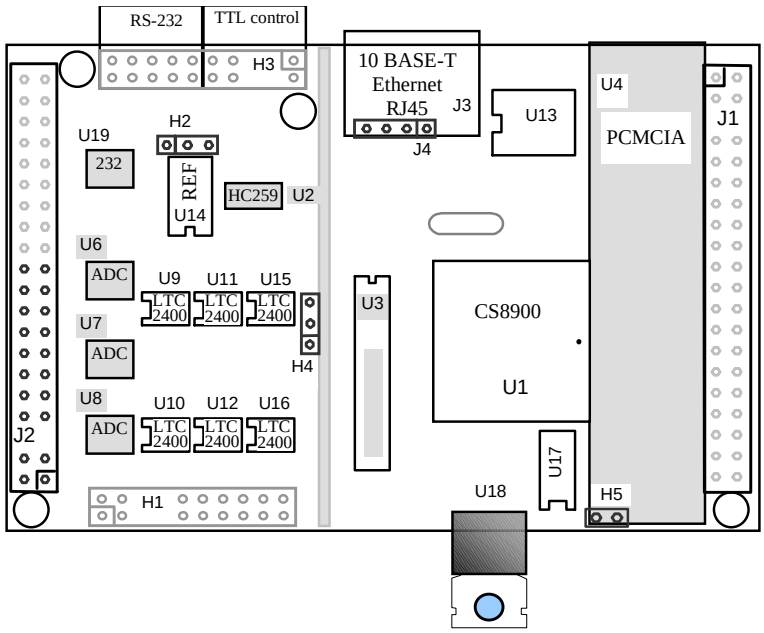
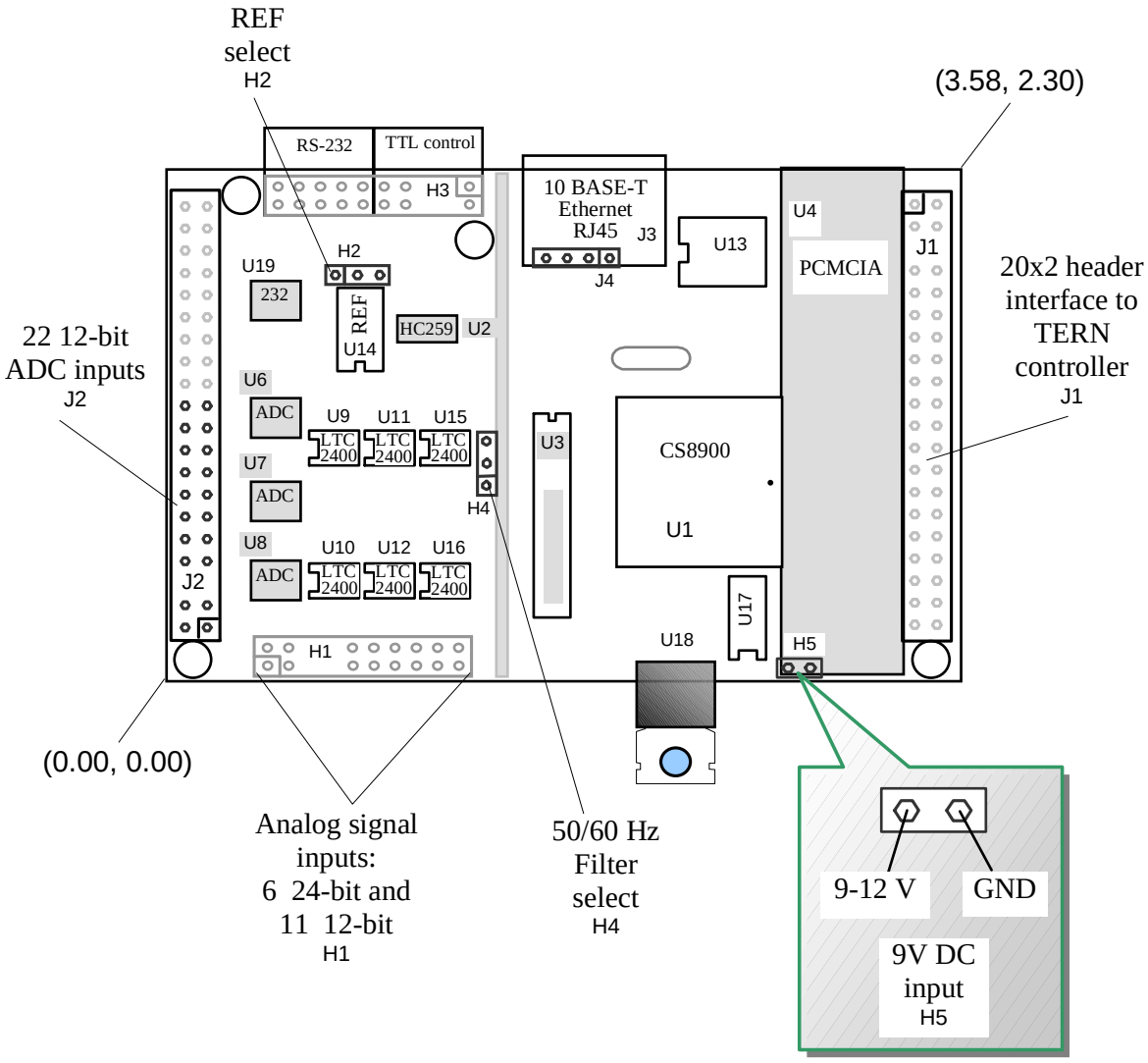


Figure 1.3 Physical layout of MemCard-A

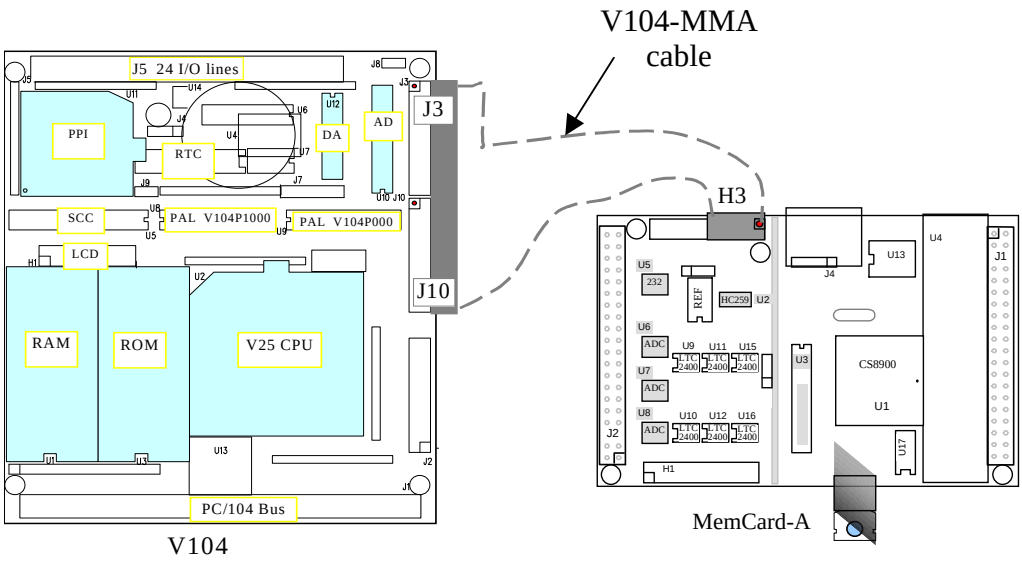
Appendix A: MemCard-A layout

All dimensions are in inches.
The MemCard-A measures 3.6 x 2.3 inches. Its layout is shown below.



Appendix B: Interface to V104

The following diagrams illustrate how to connect the V104 to the MemCard-A via TTL pins, using a cable.



V104

J3

1

GND

VCC

20

J10

1

P12

P27

P25

P24

PT7

PT6

P15

P06

20

20

VCC GND

/RST=P12 A0=P27

/259=P25 A1=P24

D0=P15 A2=P06

D24=PT7 D12=PT6

1

H3

MemCard-A

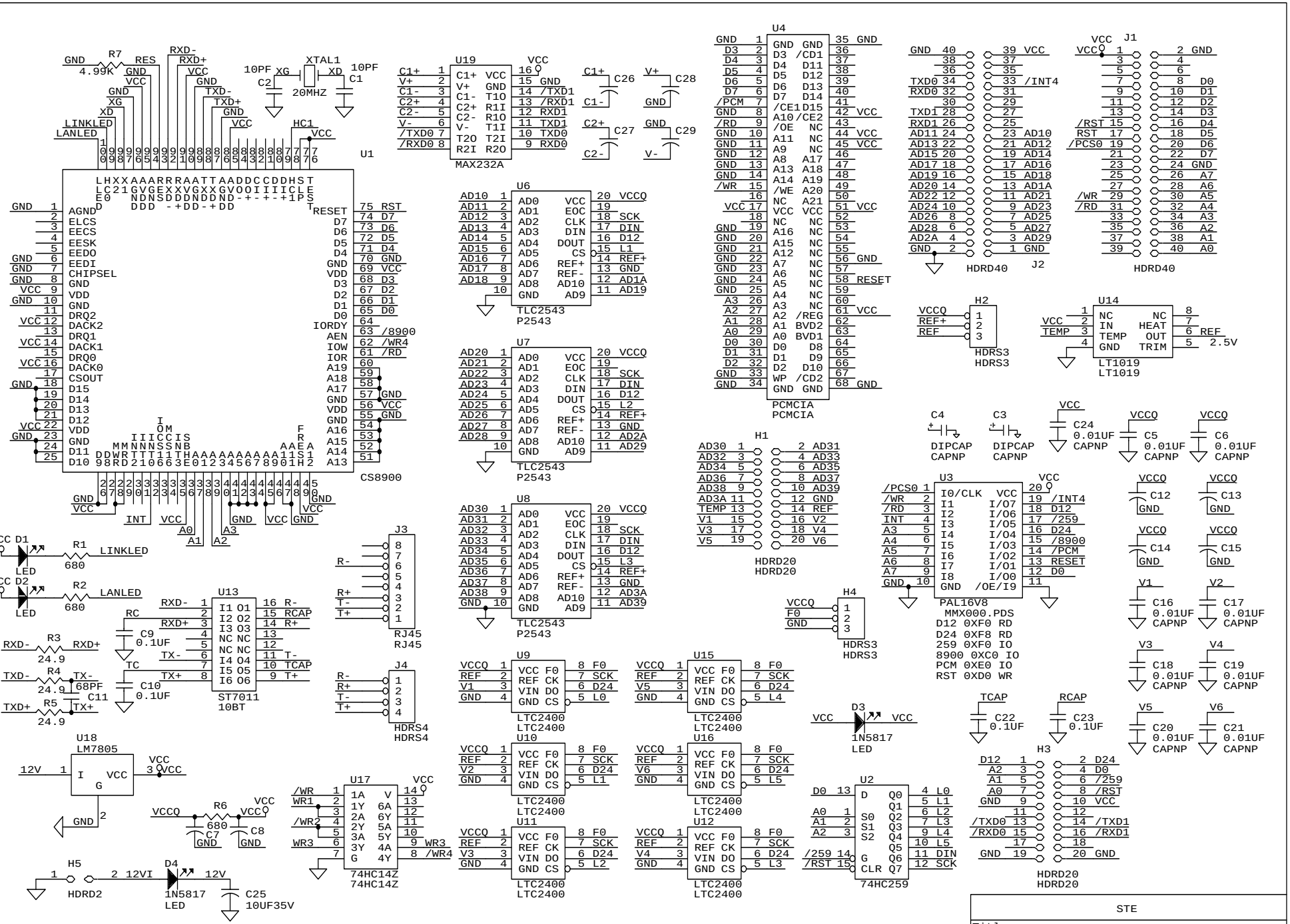
Appendix C: MemCard-A Code

```
/*****************************************************************
mm_id.c
Test SanDisk FlashDISK 68-pin PCMCIA ATA card ID number 9-23-1999
There are 512 bytes “Identify Drive Information” stored within each card
Using read_id(sec_buf);
reads it into 512 bytes sec_buf[512]
Refer to SDP3B FlashDisk Product Manual page 61, Table 6-3
See www.sandisk.com and www.devcorner.net for
*****************************************************************/
#include “ae.h”           /* A_Engine initialization */
#include “mma.h”
unsigned int i;
unsigned char sec_buf[512];

void main(void)z
{
ae_init();       /* A-Engine initialization */
for(i=0;i<512;i++){
sec_buf[i]=0;
  }

software_reset(); // Software reset

//
// Reads Card Identify Drive Information of 512 bytes into sec_buf
// By default:
//    sec_buf[0]=0x8a
//    sec_buf[1]=0x84
// Number of sectors per card   are stored in:
//    sec_buf[14]=MSW_l, sec_buf[15]=MSW_h,
//    sec_buf[16]=MSW_l, sec_buf[17]=MSW_h,
//
//Total number of sectors addressable in LBA Mode are stored in:
//    sec_buf[123], sec_buf[122], sec_buf[121], and sec_buf[120],
//    Example:
//    For a 4 MB card, there may be only 0x1c00=7168 sectors available:
//    sec_buf[123]=0; sec_buf[122]=0; sec_buf[121]=0x1c; sec_buf[120]=0;
//    For a 110 MB card, there may be only 0x34800=215040 sectors avilable:
//    sec_buf[123]=0; sec_buf[122]=3; sec_buf[121]=0x48; sec_buf[120]=0;
//
read_id(sec_buf);
// set breakpoint below, use Watch sec_buf, sec_buf[0], sec_buf[1], ...
}
```



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