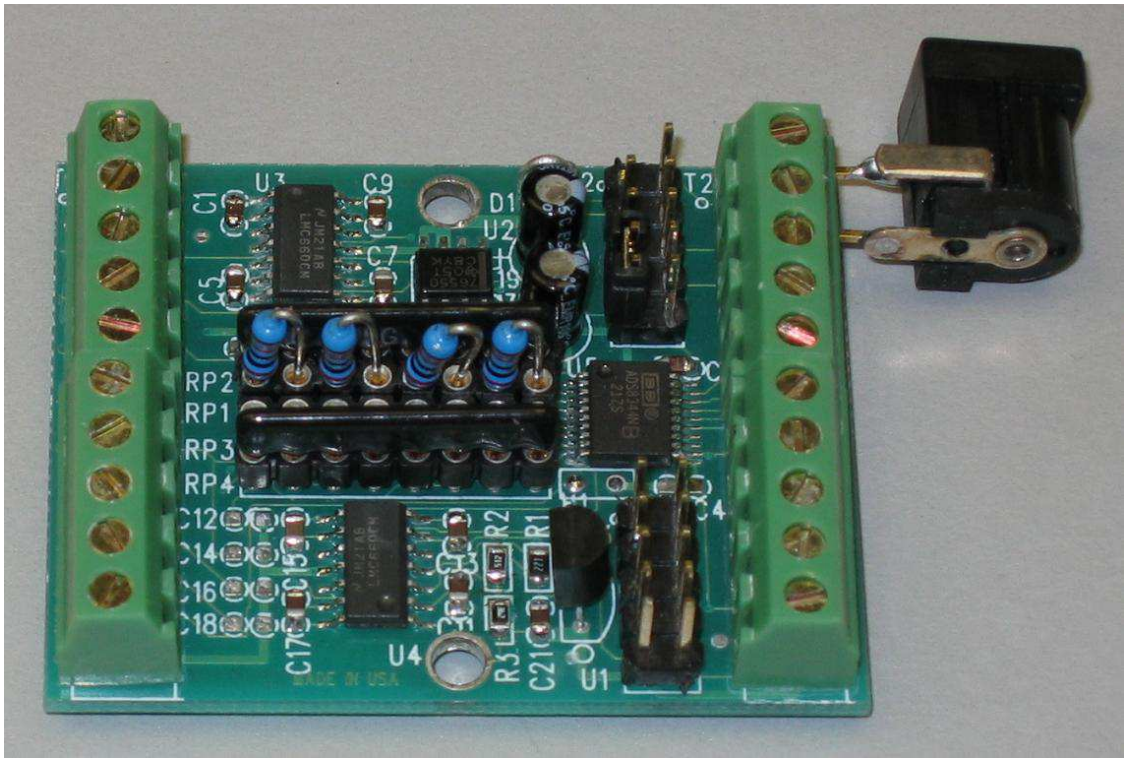
OPA™

Low cost, 8 channel, 16-bit ADC with operational amplifiers providing
+-10V signal conditioning, driven by 3 TTL I/Os.



Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

The OPA is designed for adding 16-bit ADC inputs and analog signal conditioning to embedded controllers. The OPA has eight operational amplifiers with high input impedance, which convert industry standard +-10V analog input signals to 0-4V analog signals. The 0-4V signals are then directly fed into the ADC, external or on-baord. Many ADCs on TERN controllers accept only 0-5V. The OPA offers analog signal conditioning to convert +-10V signals into 0-4V. An optional 8 channel, 16-bit ADC (ADS8344, TI) can be installed on-board. The ADC offers 8 single-ended or 4 differential inputs with 65536 counts of resolution at up to 10KHz sample rate. Any TERN embedded controller can interface to the OPA's 16-bit ADC via two TTL outputs (CLK, DIN) and one TTL input (DOUT). For application requiring additional analog inputs, multiple OPAs can interface to a signal TERN controller by sharing common CLK and DIN signals and a unique DOUT signal for each OPA. For example, 2 OPAs, providing 16 analog inputs would require only 2 TTL outputs and 2 TTL inputs. Sample programs are available for interfacing with any TERN controller. All +-10V inputs are connected to the OPA using screw terminals. The TTL interface can be connected using screw terminals or pin headers. A 4.096V precision reference with low temperature coefficient (100ppm/C^{o}) is on-baord and available externally via screw terminal. The OPA can be powered by an unregulated 5.1-9 volt supply with on-board regulator, or an externally regulated VCC (+5V). Gain modification is supported to customize analog input range.

1.2 Features

Standard Features

- Dimensions: 2.0" x 1.6"
- Power input: +5.1 - 9V unregulated DC with on-baord low drop regulator
  +5V regulated DC
- 4.096V 100ppm/C^{o} precision referenc
- 8 operational amplifiers with high impedance inputs
- Signal conditioning converts +-10V to 0-4V

Optional Features

- 8 channel 16-bit ADC (ADS8344) with 3 wire TTL interface

1.3 Physical Description

The physical layout of the OPA is shown in Figure 1.1.

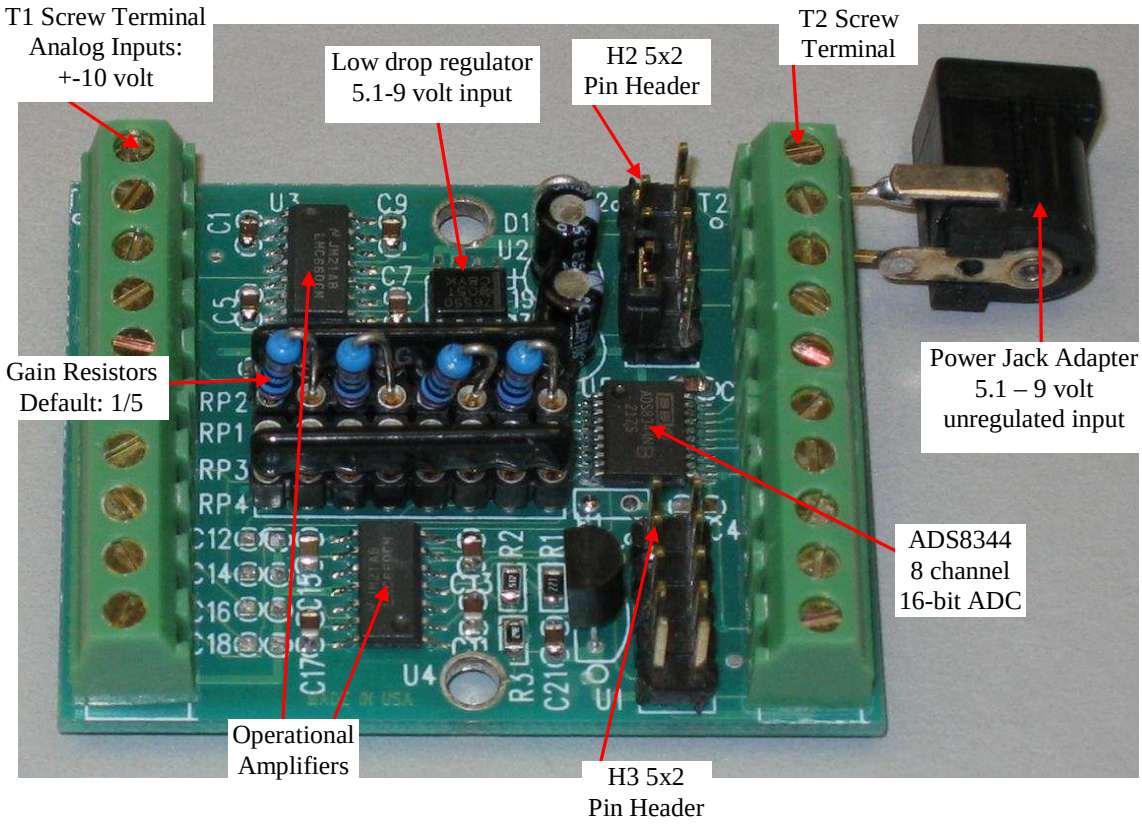


Figure 1.1 Physical layout of the OPA

1.4 Sofware

TERN provides sample code to interface the OPA's ADC with TERN controllers. The /CS signal is located at the T2 screw terminal and the H2 pin header and is tied to GND by hardware default. The DOU signal is tri-stated based on the state the /CS. With /CS high, DOU is high impedance and with /CS low, the ADC will drive an output on DOU. Because /CS is tied low by hardware default, it is necessary for DOU to not be shared with any other hardware on the driving TERN controller. TERN software drivers offer a variey of methods for interfacing to the OPA to allow for maximum flexability during application design. The OPA can be interface via CPU I/O, hardware peripheral I/Os, or expansion board I/Os (such as the P50 or the P100). In some TERN controllers, a high voltage driver (ULN2003A) can be replace with an IC resistor pack to create a TTL interface.

The OPA also allows the user to create a custom interface based upon other application demands by simply using any three TTL level I/Os and copying the interface logic of existing TERN OPA drivers from provided sample code.

There currently exists pre-built sample projects for the OPA. See **tern\186\samples\opa\opa.ide**. Source code exists in the same directory. Please read documentation in the source code to determine which source file matches the configuration in use.

1.5 Hardware

The OPA consists primarily of 4 on-bard ICs and one precision reference. This includes two 4-channel operationl amplifiers (LM669), one low-drop regulator (TPS76550), and one 8 channel 16-bit ADC. The ADC data sheet (ADS8344.pdf) can be found in the **tern_docs\parts** directly

1.5.1 16-bit ADC (ADS8344)

The ADS8344 is an 8 channel, 16-bit sampling analog-to-dgital converter with a synchronous serial interface. Input voltage range is 0 – Vref, where Vref is set by hardware default to 4.096 volts via LM404 precision reference, located at U1. The ADC requires a three wire TTL level interface (two inputs and one output, which translates to two outputs and one input from the host controller). All control signals are available at screw terminals or pin headers on the OPA.

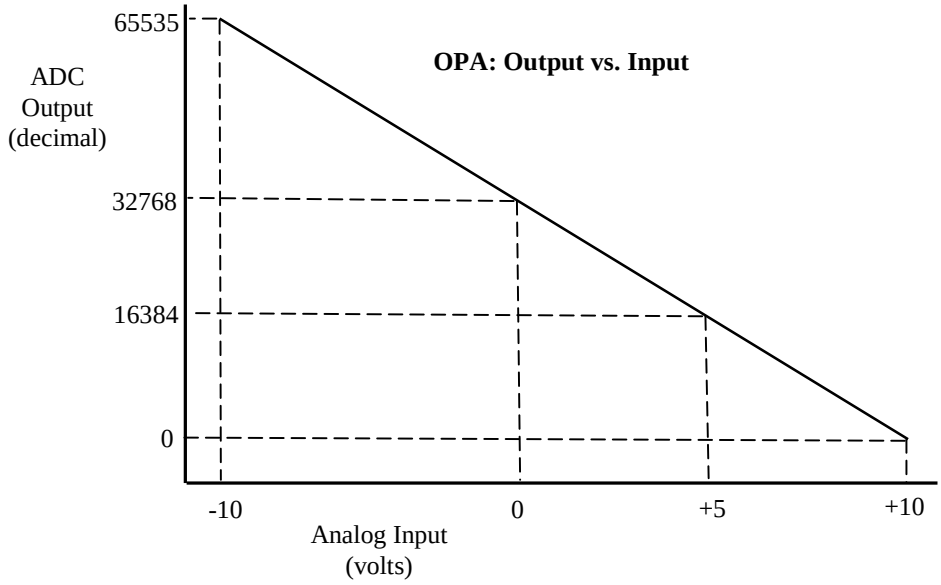
The ADC digital data output communicates with a host through a tri-state serial output (DOU). If /CS is low, the ADS will drive an output on DOU. By hardware default, /CS is tied low, activating the output on DOU. For this reason the DOU signal from the host cannot be shared with any other hardware.

The ADS8344 supports 8 single-ended or 4 differential inputs. By default, TERN software drivers use single ended input, but can be easily modified to support differential input by modifying the control byte written to the ADS8344 via DIN. Refer to the ADS8344 data sheet for details on control byte.

All ADS8344 signals are routed to external connections on the OPA, yet it is only necessary to use three. The Table below gives a summary.

/CS	Tied to GND	Active Low. Tied to GND by hardware default. H2.7 and T2.6
DIN	Output from Host	Data In. Carries control byte into ADC. Determines ADC behavior. See sample code. H2.4 and T2.4
DOU	Input to Host	Serial Data Out. Carries conversion result back to host. H2.5 and T2.5
BSY	Not Implemented	Ouput. BSY is low while reading the control byte and during conversion. H2.6 and T2.7
CLK	Ouput from Host	Clocks the serial input on DI and serial output on DOU. H2.3 and T2.3
REF	Set by hardware	Upper reference voltage. Ties to LM404 precision reference. T2.9
COM	Set by hardware	Lower reference voltage. Tied to GND by hardware default.
5V	VCC	VCC. Can be supplied by host controller, or generated by on-baord regulator. H2.10 and T2.8
GND	GND	Ground. H2.9 and T2.10

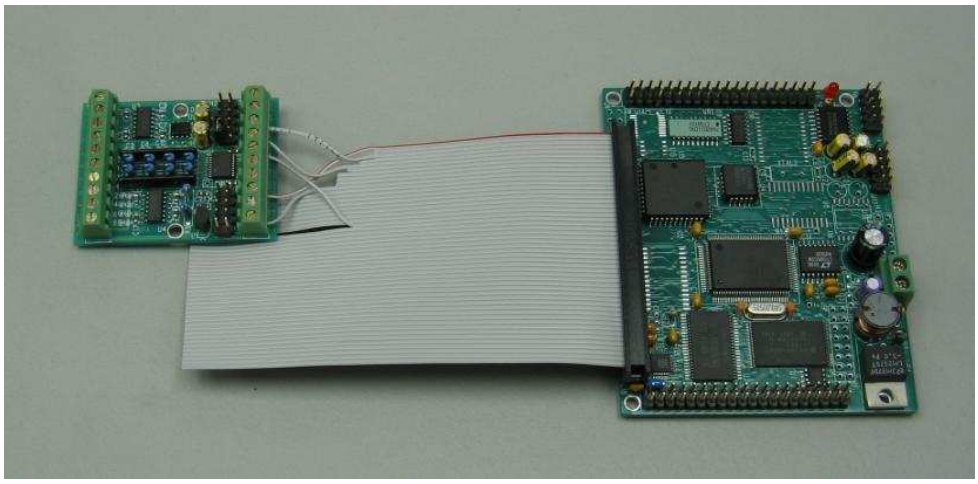
For any additional information on the ADS8344, refer to the schematic at the end of this manual, the data sheet in the **tern_docs\parts** directory of the installation CD, or the host controller technical manual.



The above figure shows the digital decimal output versus analog input for the OPA.

1.5.2 LMC660 Operational Amplifier

Two four-channel LMC660 operational amplifiers are installed on-baord. They provide signal conditioning necessary to support +-10V analog inputs. The inputs are routed to the T1 screw terminal. The outputs from the operational amplifiers are routed to the H3 pin header. This header is used when the ADS8344 is not installed and the OPA is used solely for signal conditioning for an external ADC. They amplifier outputs are also routed to the analog inputs when the ADS8344 is installed. It is necessary to note that when the ADS8344 is installed, the use cannot simple supply the ADC with analog input directly at the H3 header (between the outputs of the amplifiers and inputs of the ADC). This will cause conflict between the outputs of the amplifiers and the external analog source. The amplifiers use VCC for supply voltage and use a deault gain of 1/5 to support the +-10V inputs. Gain resistors can be modified to support alternate analog intput ranges. The OPA is shown driven by the PPI chip on the A-Engine86-P below.



1.6 Headers and Connectors

H3 Header			
AD0	1	2	AD1
AD2	3	4	AD3
AD4	5	6	AD5
AD6	7	8	AD7
GND	9	10	5V

H2 Header			
V+	1	2	GND
CLK	3	4	DIN
DOU	5	6	BSY
/CS	7	8	REF
GND	9	10	5V

T1 Screw Terminal	
1	AN0
2	AN1
3	AN2
4	AN3
5	AN4
6	AN5
7	AN6
8	AN7
9	COM
10	GND

T2 Screw Terminal	
1	V+
2	GND
3	CLK
4	DIN
5	DOU
6	/CS
7	BSY
8	5V
9	REF
10	GND

The T1 screw terminal provides the +-10V inputs. When the ADS8344 is not installed (OPA used only as analog signal conditioning), the outputs of the operational amplifiers can be taken from the H3 pin header and sent to an external ADC, such as on a TERN controller.

Appendix A: Application Notes

The OPA can be implemented by any TERN controller using a variety I/O lines. In each case only 3 discrete digital I/Os are needed and TERN provides sample drivers for most TERN controllers. In addition, the user can create their own driver based on any I/Os they chose by simply following the design of any pre-existing OPA driver.

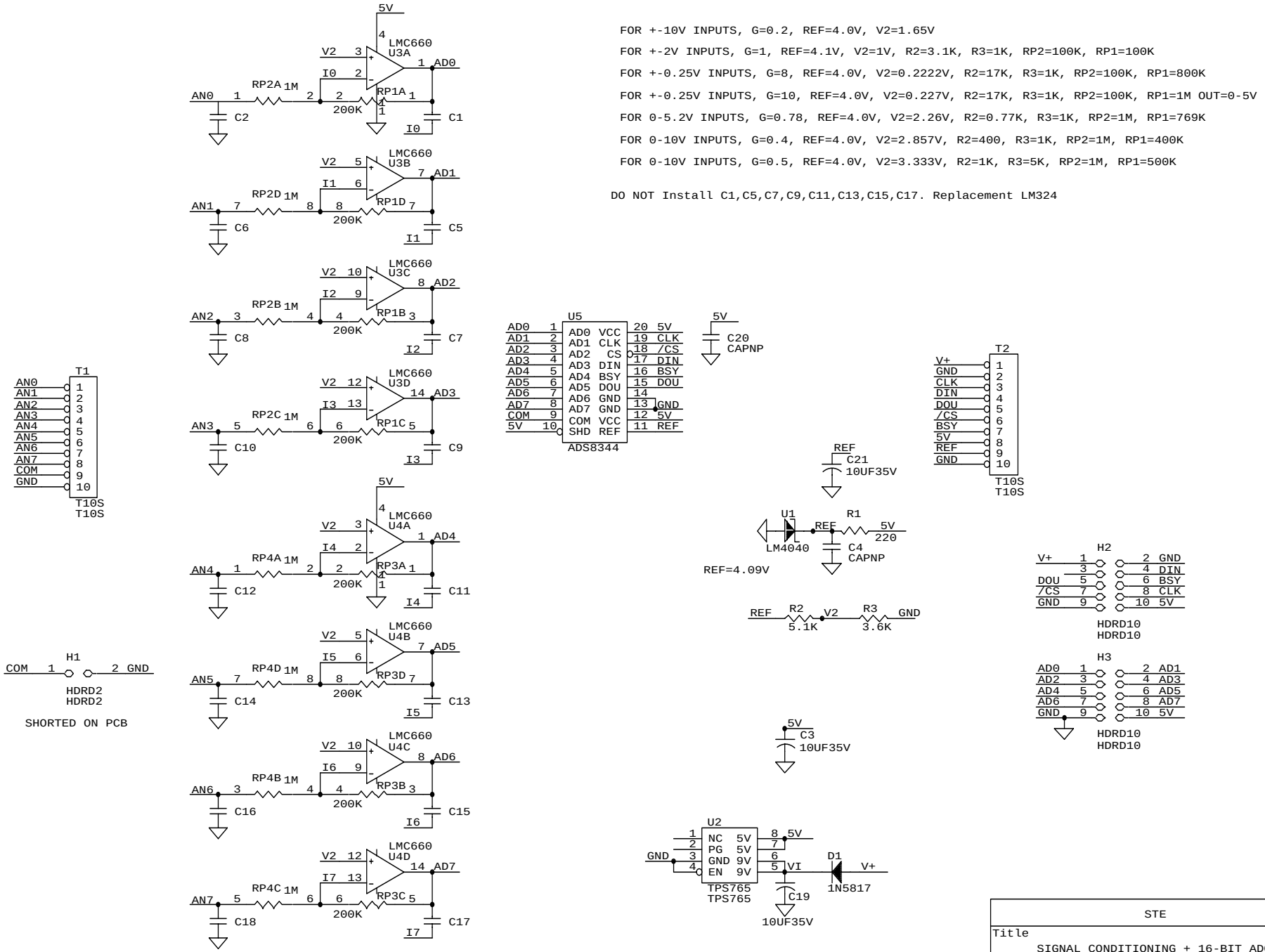
However, with the 'R' based boards (R-Engine, RD, RA, RM, and RL) there are additional considerations to take into account. Because the PIOs from the RDC1100 and Am186ER are 3.3V lines, the ADS8344 can misread logic highs as logic lows, missing bits. This only starts to occur at a certain cable length. More specifically, with a short enough cable (connecting the controller to the OPA), the ADS8344 will not miss bits, but as the cable length is increased, the risk of missing bits is also increased.

To complete a conversion on a certain channel with the ADS8344, the user must clock in an 8-bit control byte into the Data In pin of the ADS8344 (see \tern_docs\parts\ads8344.pdf for details on control byte). This control byte contains information on which channel to convert, single-ended or differential, etc. When the ADS8344 misses bits, the CLOCK and/or the Data In line misses a logic high as low and results in the ADS8344 receiving a garbage control byte. As a result, the ADS8344 will return a value of 0x0000 for the channel being read.

When creating a driver for the OPA using 'R' based boards, avoid using the 3.3V PIO lines whenever possible. If it becomes unavoidable, ensure that the cable connecting the host controller and the OPA is very short to avoid missing bits. It is important to note the Data Out signal (going from the OPA to the host controller) is immune from missing bits.

Refer to tern\186\samples\rl\rl_opa.c for an example of how to implement the OPA with an 'R' based board without using 3.3V I/O lines. It uses two I/Os from the 82C55 PPI, which are 5V I/O lines, to eliminate missing bits. This method could be used with other 'R' based boards.

When using 3.3V I/O lines, cables of 3 inches have been tested and are 100% free of missing bits. When using 3.3V I/O lines, cables of approximately 9 inches have been tested and DO miss bits.


FOR +-10V INPUTS, G=0.2, REF=4.0V, V2=1.65V
FOR +-2V INPUTS, G=1, REF=4.1V, V2=1V, R2=3.1K, R3=1K, RP2=100K, RP1=100K
FOR +-0.25V INPUTS, G=8, REF=4.0V, V2=0.2222V, R2=17K, R3=1K, RP2=100K, RP1=800K
FOR +-0.25V INPUTS, G=10, REF=4.0V, V2=0.227V, R2=17K, R3=1K, RP2=100K, RP1=1M OUT=0-5V
FOR 0-5.2V INPUTS, G=0.78, REF=4.0V, V2=2.26V, R2=0.77K, R3=1K, RP2=1M, RP1=769K
FOR 0-10V INPUTS, G=0.4, REF=4.0V, V2=2.857V, R2=400, R3=1K, RP2=1M, RP1=400K
FOR 0-10V INPUTS, G=0.5, REF=4.0V, V2=3.333V, R2=1K, R3=5K, RP2=1M, RP1=500K
DO NOT Install C1,C5,C7,C9,C11,C13,C15,C17. Replacement LM324
T1
T10S
H1
HDRD2
SHORTED ON PCB
LMC660
U3A
U3B
U3C
U3D
U4A
U4B
U4C
U4D
RP1A
RP1B
RP1C
RP1D
RP2A
RP2B
RP2C
RP2D
RP3A
RP3B
RP3C
RP3D
RP4A
RP4B
RP4C
RP4D
1M
200K
U5
ADS8344
C20
CAPNP
C21
10UF35V
U1
LM4040
R1
220
C4
REF=4.09V
R2
5.1K
R3
3.6K
T2
H2
HDRD10
H3
U2
TPS765
C19
D1
1N5817
C3
STE
SIGNAL CONDITIONING + 16-BIT ADC
OPA.SCH
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