P100™

Expansion board with 100+ I/Os, 2 quadrature drivers

Technical Manual

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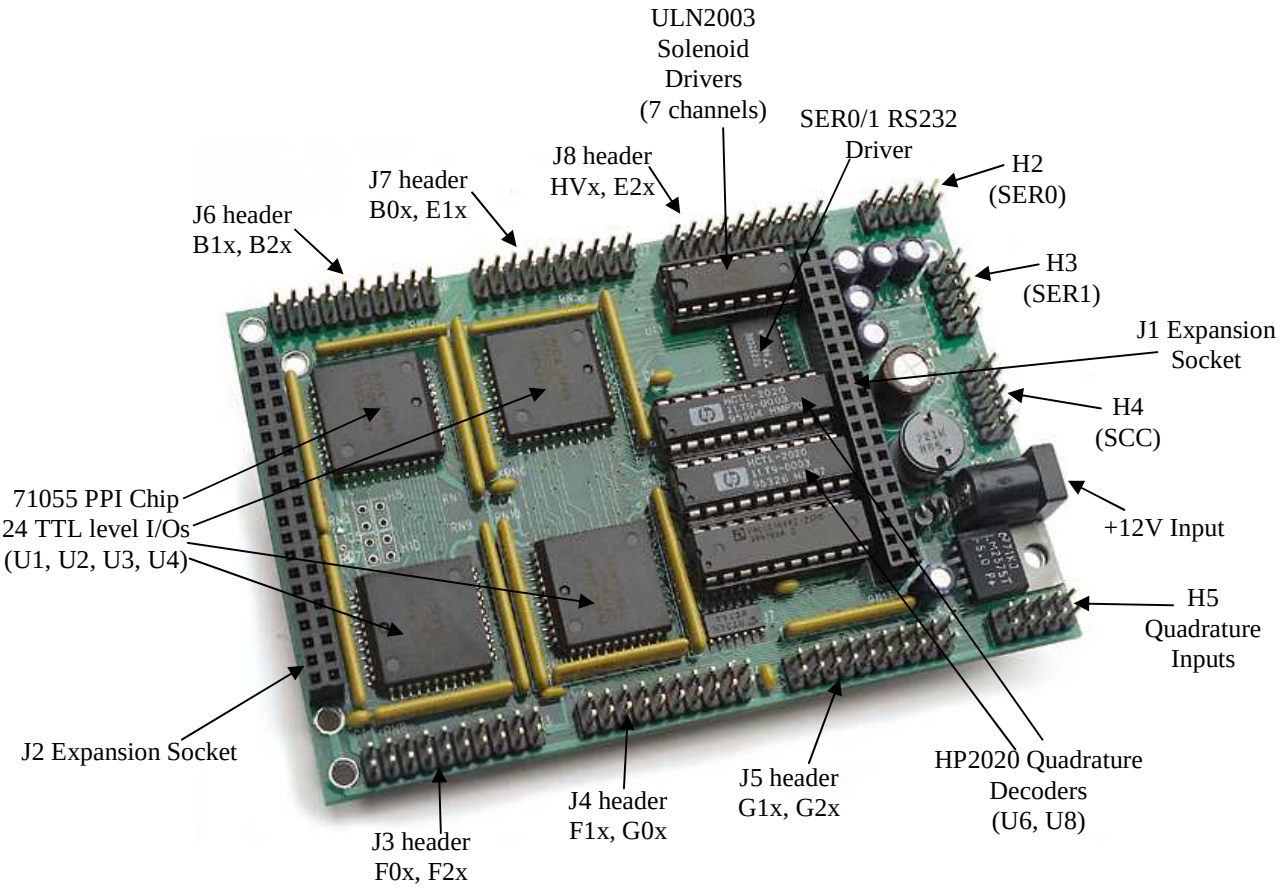
Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

Measuring 4.4 by 2.5 by 0.5 inches, the ***P100*** offers a total of 100 TTL I/O lines expansion to any of the TERN Engine boards (A-Engine, A-Engine86, i386-Engine, R-Engine, 586-Engine). The versatility of the ***P100*** allows the use of 24x4 TTL-level I/O, 7 high voltage solenoid driving output plus 2 channels of quadrature decoders (HP2020). The ***P100*** is the perfect expansion board for applications where large number I/Os and low cost are a concern.

Four PPIs (82C55) provide 96 I/O lines with 7 solenoid drivers which are capable of sinking 350 mA at 50V per line, and they can directly drive solenoids, relays, or lights.
Two channels of RS-232 drivers, one optional 3rd RS-232/485 driver, and a 5V regulator are on-board. With the default 5V linear regulator, the ***P100™*** requires 8.5V to 12V DC power input. An optional switching regulator can be installed to provide high efficiency regulation without generating heat for using DC power input up to 35V.
The P100 must be driven by a TERN Engine controller, including AE/AE86/IE/RE/5E.



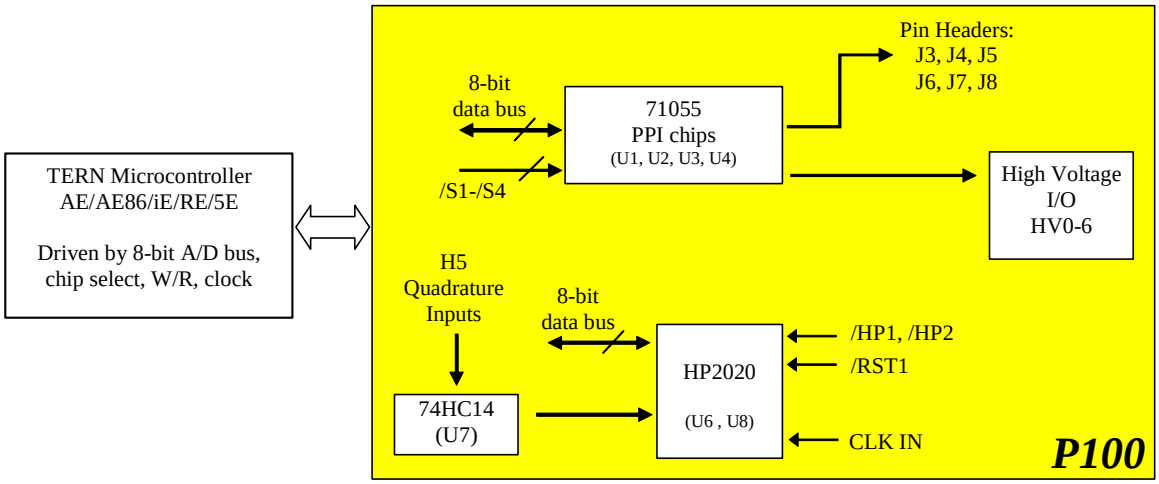


Figure 1.1 Functional block diagram of the P100

1.2 Features

- 4.4 x 2.9 x 0.5 inches
- Power consumption: < 150 mA at 9V-30V
- 24x4 TTL I/O lines from 4 PPIs, 7 solenoid drivers
- 2 quadrature decoders (HP2020) for motion control*
- Standard 5V linear regulator (9-12V unregulated input)
  Optional 5V switching regulator (9-30V unregulated input)
- RS-232 and RS-485 drivers
- Driven by ***A-Engine™, A-Engine86™, i386-Engine™, R-Engine™, 586-Engine™*** or other TERN controllers with custom hardware modification.

1.3 Physical Layout

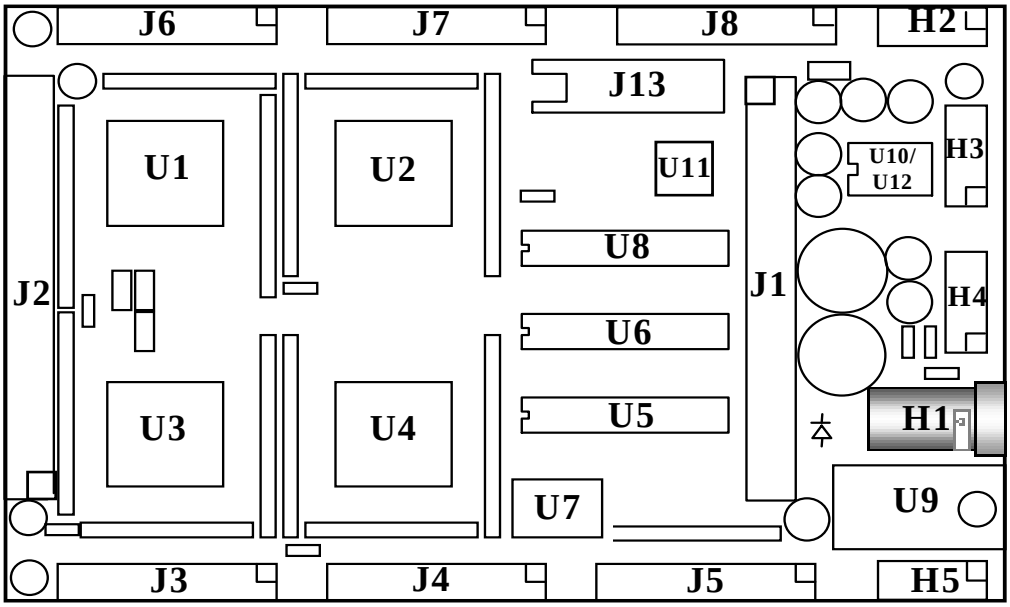


Figure 1.2 Physical layout of the P100

Chapter 2: Installation

2.1.1 Connecting the P100 and a Engine controller to the PC

The following diagram (Figure 2.1) illustrates the connection between the P100 and the PC via a serial cable (Debug Serial Cable, provided with EV-P or DV-P Kit).

An Engine controller must be installed on the P100 via J1 and J2 headers before power on. For example, below shows an R-Engine installed on the P100. It communicates through SER0 by default for debugging and application development. Install the 5x2 IDC connector on the SER0 header (H2). ***IMPORTANT:*** *Note that the* ***red*** *side of the cable must point to pin 1 of the H2 header.* The DB9 connector should be connected to one of your PC's COM Ports (COM1 COM2).

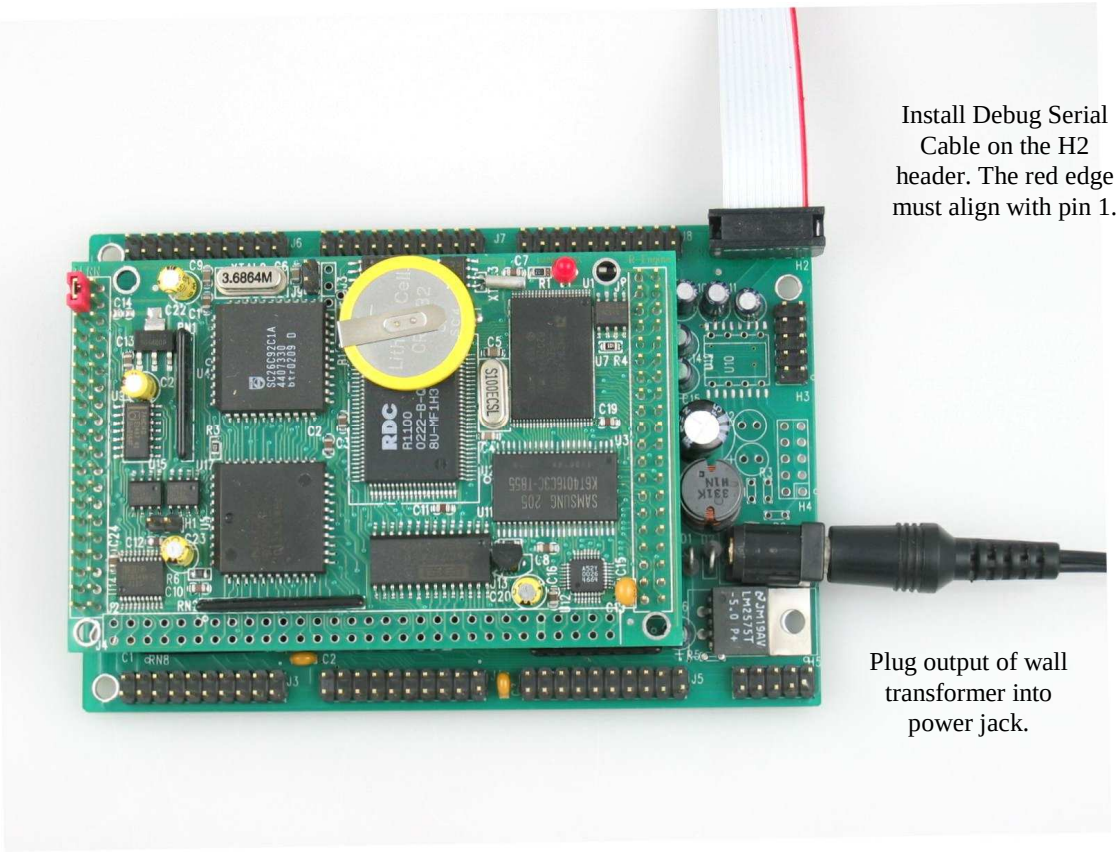
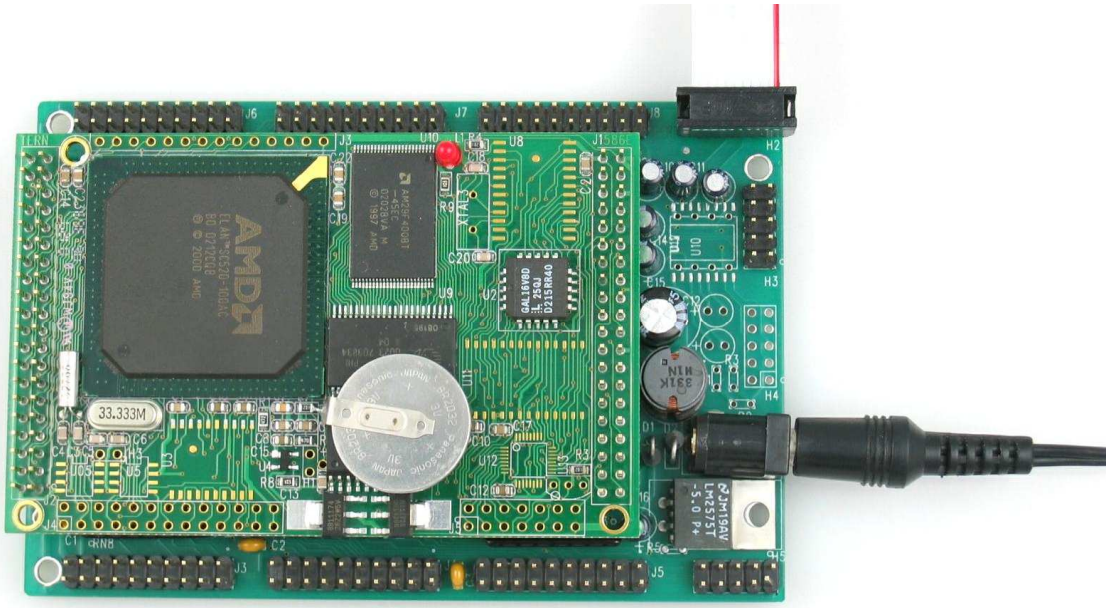


Figure 2.1 Connecting the P100 to the PC

Additional installation diagrams of the P100 with the 586-Engine and the A-Engine, respectively.



Chapter 3: Hardware

3.1 Engine controllers

The P100 must be driven by an "Engine controller", such as the A-Engine, A-Engine86, i386-Engine, R-Engine, or 586-Engine. The "Engine" installs on top of the P100 via 20x4 pin headers J1 and J2, and can be secured by two #4-40 mounting screws.

3.2 Serial Ports Drivers

The P100 can provide up to 3 channels RS-232/485 drivers. By default two RS-232 drivers ready for the two asynchronous serial channels from the installed Engine controller via 20x2 pin header J1 and J2. One optional 3rd RS232 or RS485 driver can be installed to support the UART SCC2691 on the Engine.

The default debug serial port SER0 is routed at H2; SER1 at H3 and SCC port at H4.

3.3 I/O Mapped Devices

3.3.1 I/O Space

External I/O devices can use I/O mapping for access. You can access such I/O devices with ***inportb(port)*** or ***outportb(port,dat).*** These functions will transfer one byte of data to the specified I/O address.

The table below shows more information about I/O mapping, selected by /CS6=J1.19:

I/O space	Select Signal	Location	Usage
0x80-0x83	/HP1	U6 pin 4	HP2020 U6
0x84-0x87	/HP2	U8 pin 4	HP2020 U8
0x88-0x8B	/S1	U1 pin 7	/S1 for PPI1
0x8C-0x8F	/S2	U2 pin 7	/S2 for PPI2
0x90-0x93	/S3	U3 pin 7	/S3 for PPI3
0x94-0x97	/S4	U4 pin 7	/S4 for PPI4
0x98-0x9B	/RTS1	U6 pin 7	Reset HP2020 U6
0x9C-0x9F	/RTS2	U8 pin 7	Reset HP2020 U8

3.3.2 Programmable Peripheral Interface (82C55A)

U1-U4 PPIs (82C55, or uPD81055L) are low-power CMOS programmable parallel interface units for use in microcomputer systems. They each provide 24 I/O pins that may be individually programmed in two groups of 12 and used in three major modes of operation.

In MODE 0, the two groups of 12 pins can be programmed in sets of 4 and 8 pins to be inputs or outputs. In MODE 1, each of the two groups of 12 pins can be programmed to have 8 lines of input or output. Of the 4 remaining pins, 3 are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

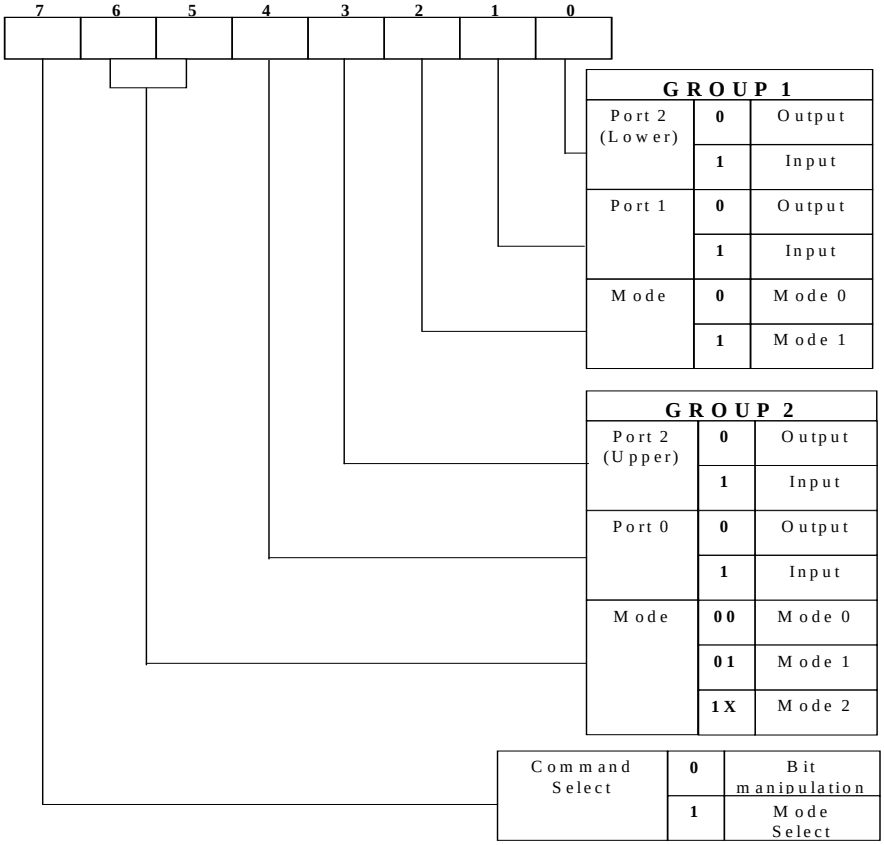


Figure 3.1 Mode Select Command Word

P100 maps U1, the PPI1 82C55/uPD71055, at base I/O address PPI1=0x??88.

P100 maps U2, the PPI1 82C55/uPD71055, at base I/O address PPI2=0x??8C.

P100 maps U3, the PPI1 82C55/uPD71055, at base I/O address PPI3=0x??90.

P100 maps U4, the PPI1 82C55/uPD71055, at base I/O address PPI4=0x??94.

Use PPI1 as example, all ports/registers are offsets of this I/O base address.

The Command Register = PPI1+3; Port 0 = PPI1; Port 1 = PPI1+1; and Port 2 = PPI1+2.

The following code example will set all ports to output mode:

```
outportb(PPI1+3,0x80); /* Mode 0 all output selection. */
outportb(PPI1+0,0x55); /* Sets port 0 to alternating high/low I/O pins. */
outportb(PPI1+1,0x55); /* Sets port 1 to alternating high/low I/O pins. */
outportb(PPI1+2,0x55); /* Sets port 2 to alternating high/low I/O pins. */
```

To set all ports to input mode:

```
outportb(PPI1+3,0x9f);     /* Mode 0 all input selection. */
```

You can read the ports with:

```
inportb(PPI1+0); /* Port 0 */
inportb(PPI1+1); /* Port 1 */
inportb(PPI1+2); /* Port 2 */
```

This returns an 8-bit value for each port, with each bit corresponding to the appropriate line on the port.

There are a total of 24x4 TTL level I/O pins are free to use for your applications. These I/O lines are specified as 4 mA driving current capability. Seven PPI TTL lines (E00-E06) are used to drive the U13 solenoid drivers.

See schematics for PPI connection headers of J3 to J8.

The I/O addresses used above are for example only. Please refer to the correct sample based on the host Engine.

3.3.3 HCTL2020

Two quadrature decoder/counter interface chips, (HCTL2020, Hewlett Packard, U08 and U06) can be installed. The quadrature decoder is used to interface incremental motion encoders with the microprocessor system or to improve system performance for digital closed-loop motion control systems. The HCTL2020 includes a quadrature decoder, a 16-bit counter, and an 8-bit bus interface. It features full 4x decoding, up to 14 MHz clock operation, high noise immunity due to the use of Schmitt-trigger inputs and digital noise filters, quadrature decoder output signals, up/down signal, count signals, and cascade output signal. Many types of optical incremental encoder modules, such as the HEDS-9000, HEDS-9100, and HEDS-9200 from HP, can be directly interfaced to the HCTL2020.

Channel A and B signals buffered with Schmitt trigger inputs (U7, 74HC14, CHA1/2, CHB1/2) are routed at pin 5, 6, 9, and 10 on headers H5. The HCTL2020 has built-in filters, which allow reliable operation in noisy environments.

Two software functions (found in **`c:\tern\186\samples\p100\p100_hp.c`**) are available to operate the quadrature decoders:

unsigned int ***p100_hp_rd***(char ch);
void ***p100_hp_reset***(char ch);

3.3.4 High-Voltage, High-Current Drivers

ULN2003 has high voltage, high current Darlington transistor arrays, consisting of 7 silicon NPN Darlington pairs on a common monolithic substrate. All channels feature open-collector outputs for sinking 350 mA at 50V, and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA sinking are allowed. U7 is the high-voltage drivers. These outputs may be paralleled to achieve high-load capability, although each driver has a maximum continuous collector current rating of 350 mA at 50V. The maximum power dissipation allowed is 2.20 W per chip at 25 degree C. The common substrate G is routed to J8 GND pins. All currents sinking in must return to the J8 GND pins (J8 pin 9, 19,20). A heavy gage(20) wire must be used to connect the J8 GND terminal to an external common ground return. K connects to the protection diodes in the ULN2003 chips and should be tied to highest voltage in the external load system. K can be connected to an unregulated on board +12V. **ULN2003 is a sinking driver not sourcing driver.** Typical application wiring is shown below.

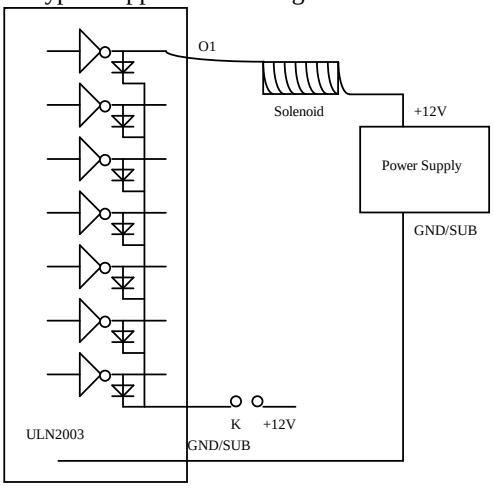


Figure 3.2 Drive inductive load with high voltage/current drives.

3.4 Headers and Connectors

3.4.1 Expansion Headers J1 and J2

Two 20x2, 0.1 spacing sockets are installed on the P100 for Engine installation. Most signals are directly routed to the Engine processor. These signals are 5V only (in some cases 3.3V signal, and 5V tolerant), and any out-of-range voltages will most likely damage the board.

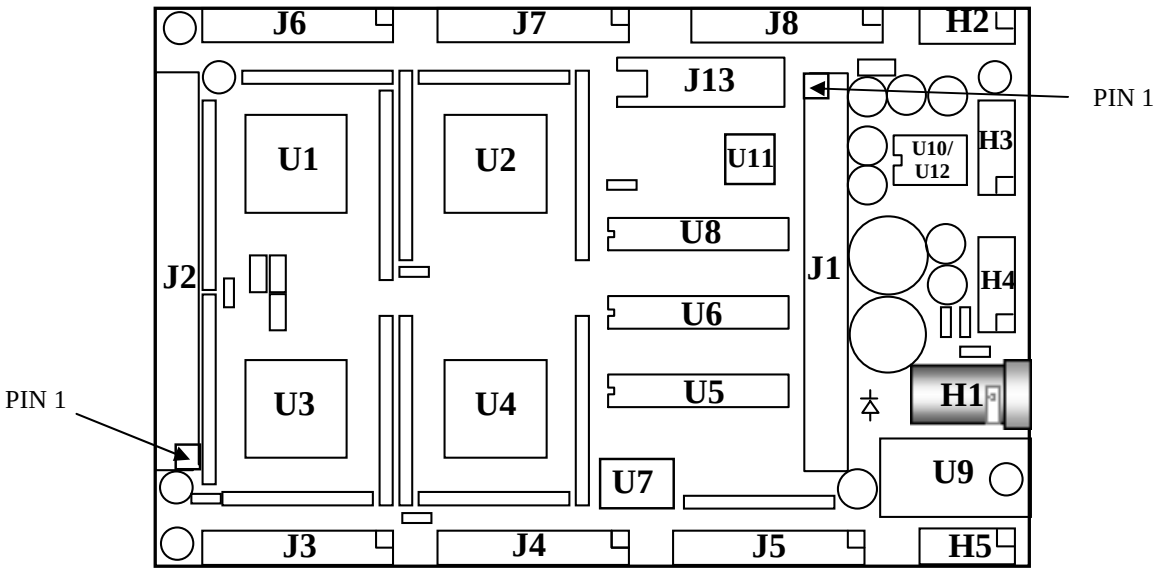


Figure 3.3 Pin 1 locations for J1 and J2

J1 Signal				*J2 Signal*			
VCC	1	2	GND	GND	40	39	VCC
MPO	3	4	TOUT2	RI1	38	37	P21
RxD	5	6	GND	P27	36	35	P37
TxD	7	8	D0	TxD0	34	33	/INT4
VOFF	9	10	D1	RxD0	32	31	/RTS1
	11	12	D2	P36	30	29	P35
	13	14	D3	TxD1	28	27	P11
/RST	15	16	D4	RxD1	26	25	DTR1
RST	17	18	D5	P34	24	23	P33
/CS6	19	20	D6	/CTS1	22	21	P32
	21	22	D7	P13	20	19	P31
	23	24	GND	P12	18	17	P30
	25	26	A7	R/W	16	15	/INT7
	27	28	A6	P10	14	13	P17
/WR	29	30	A5	P14	12	11	P16
/RD	31	32	A4	P23	10	9	TCLK2
	33	34	A3	/INT5	8	7	NMI
	35	36	A2	/INT6	6	5	P22
	37	38	A1	DSR1	4	3	P24
	39	40	A0	GND	2	1	DCD1

Table 3.1 J1 and J2, 20x2 expansion ports on the P100

Signal definitions for J1:

VCC	+5V power supply
GND	Ground
TOUT2	Intel386EX pin 91, timer2 output, 8.25 MHz maximum
RxD	data receive of UART SCC2691, U8
TxD	data transmit of UART SCC2691, U8
MPO	Multi-Purpose Output of SCC2691, U8
VOFF	real-time clock output of RTC72423 U4, open collector
D0-D7	Data bus from Host Engine to P100 devices
A0-A7	Address bus from Host Engine to P100 devices
/RST	reset signal, active low
RST	reset signal, active high
/CS6	/CS6, Intel386EX pin 2, ie_init(); set it up as I/O chip select line at address 0x8000
/WR	Intel386EX pin 35, active low when write operation
/RD	Intel386EX pin 34, active low when read operation

Signal definitions for J2:

VCC	+5V power supply, < 300 mA
GND	ground
Pxx	Intel386EX PIO pins
R/W	inverted from Intel386EX pin 30, W/R
TxD0	Intel386EX pin 131, transmit data of serial channel 0
RxD0	Intel386EX pin 129, receive data of serial channel 0
TxD1	Intel386EX pin 112, transmit data of serial channel 1
RxD1	Intel386EX pin 118, receive data of serial channel 1
P27=/CTS0	Intel386EX pin 132, Clear-to-Send signal for SER0
/CTS1	Intel386EX pin 113, Clear-to-Send signal for SER1
P11=/RTS0	Intel386EX pin 102, Request-to-Send signal for SER0
/RTS1	Intel386EX pin 110, Request-to-Send signal for SER1
/INT4-7	Schmitt-trigger buffered active low interrupt inputs
P32-35=INT0-3	active high interrupt inputs
TCLK2	timer2 clock input
NMI	Non-mask interrupt
DSR1, DCD1, RI1, DTR1	Serial port 1 handshake lines
RI1	J2 pin 38 Used as Step Two jumper

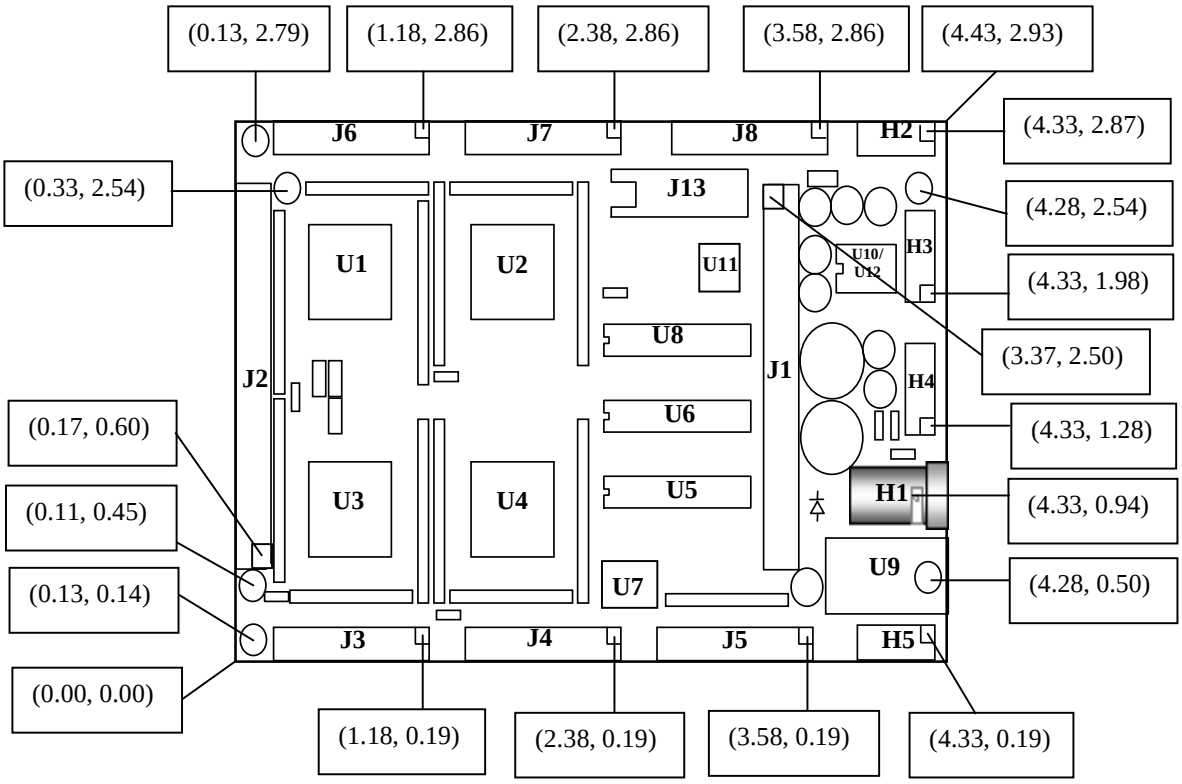
3.4.2 Jumpers and Headers

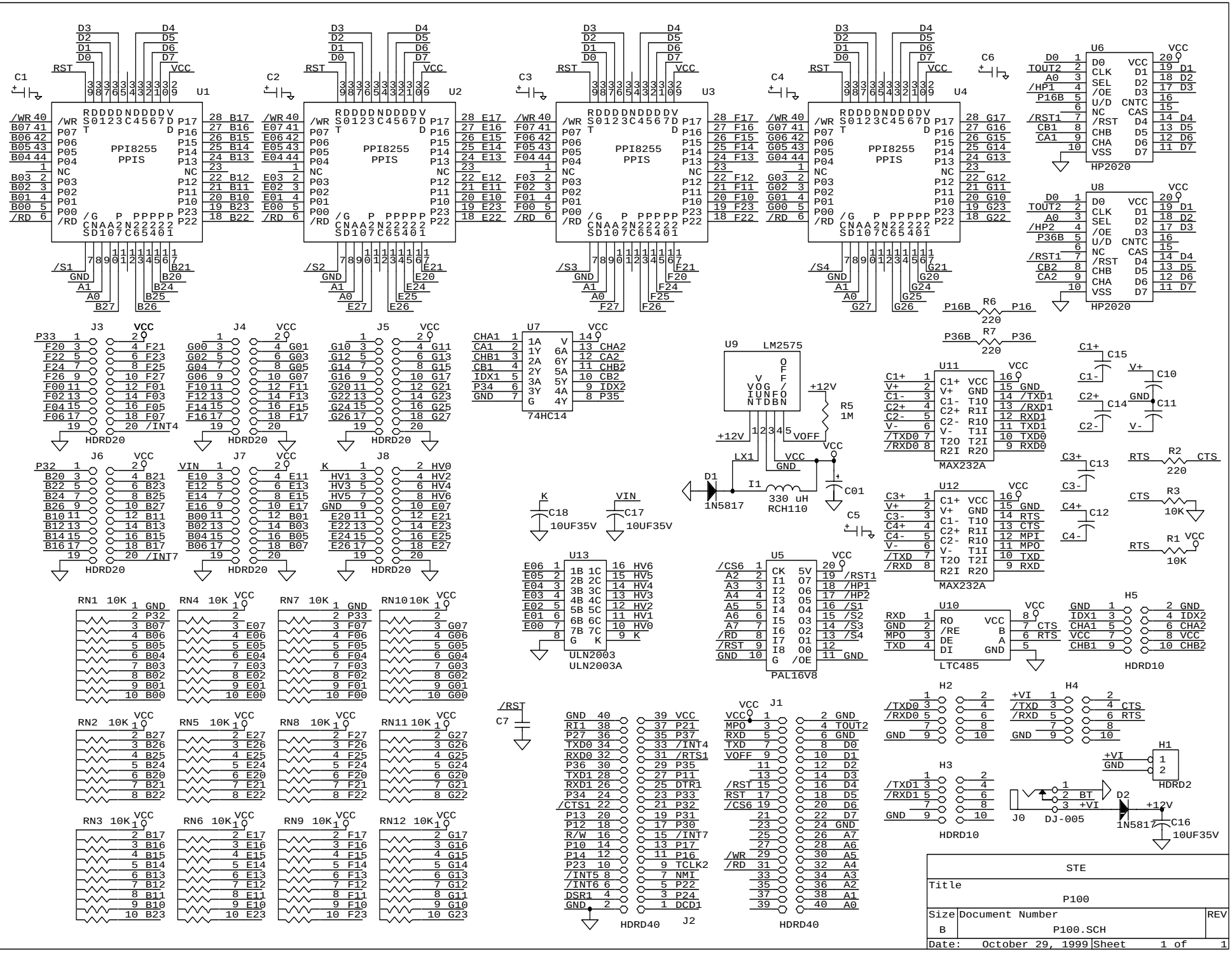
The jumpers and connectors on the P100 are listed below.

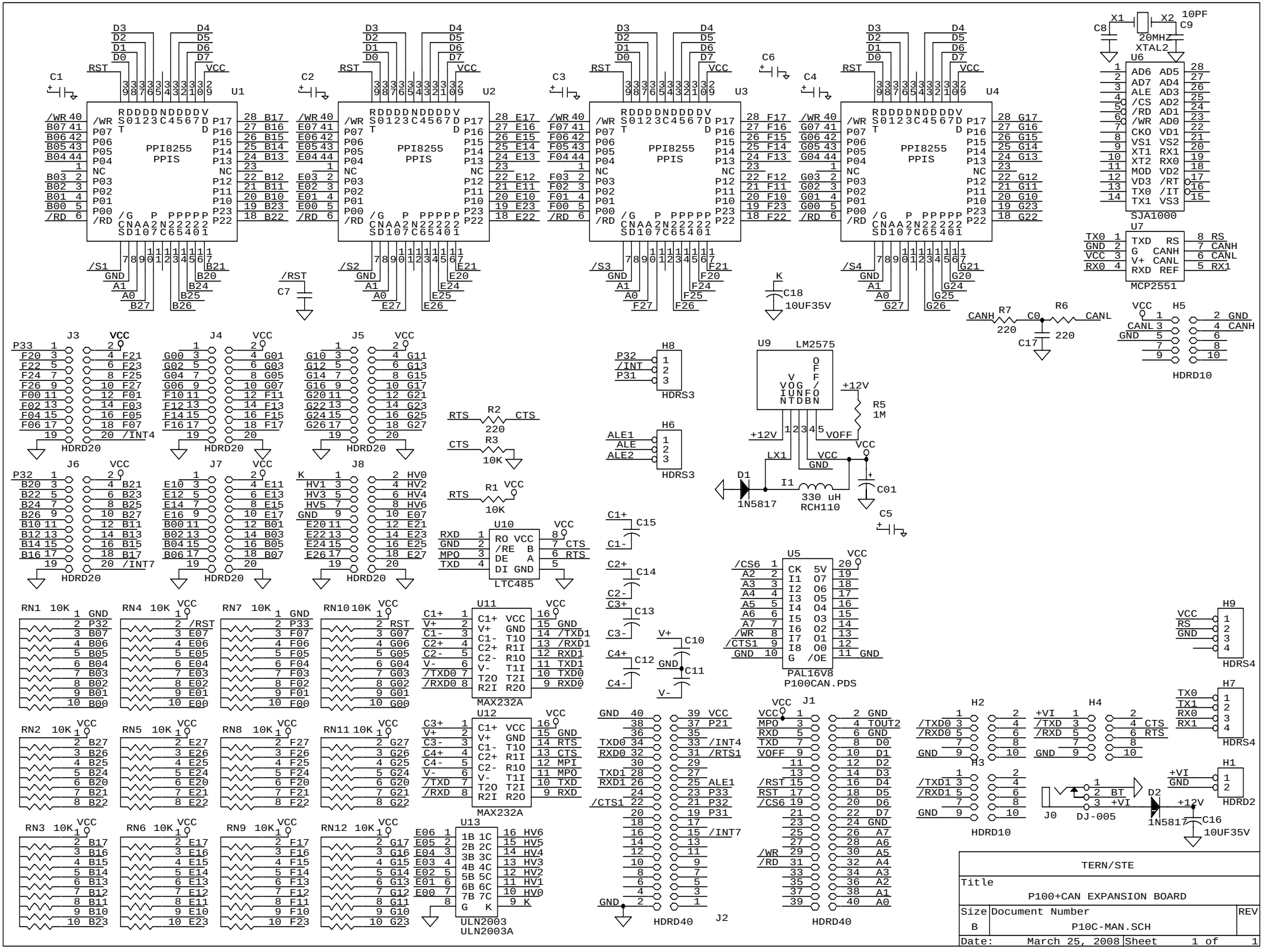
Name	Size	Function	Possible Configuration
J1	20x2	main expansion port	(same as the i386-Engine and i386-Engine-P)
J2	20x2	main expansion port	(same as the i386-Engine and i386-Engine-P)
J3	10x2	PPI TTL I/O lines	U3
J4	10x2	PPI TTL I/O lines	U3 and U4
J5	10x2	PPI TTL I/O lines	U4
J6	10x2	PPI TTL I/O lines	U1

Name	Size	Function	Possible Configuration
J7	10x2	PPI TTL I/O lines	U1 and U2
J8	10x2	HV and PPI TTL I/O lines	U2
H1	2x1	+12V power input	
H2	5x2	SER0 (DEBUG), RS232	
H3	5x2	SER1, RS232	
H4	5x2	SCC2691: RS232/485 TXD, RXD, GND	Install RS232 or RS485 driver for 3rd UART
H5	5x2	HP2020s	

Appendix: P100 mechanical dimensions




U1
U2
U3
U4
PPI8255
PPIS
SD107C65401
C1
C2
C3
C4
C6
U6
U8
HP2020
P16B
R6
220
P36B
R7
220
J3
J4
J5
J6
J7
J8
HDRD20
U7
74HC14
U9
LM2575
+12V
R5
1M
D1
1N5817
I1
330 uH
RCH110
C01
C5
C18
10UF35V
C17
10UF35V
U11
MAX232A
C15
C10
C14
C11
U12
MAX232A
R2
220
R3
10K
R1
10K
U13
ULN2003
ULN2003A
U5
PAL16V8
U10
LTC485
H5
HDRD10
RN1 10K
RN2 10K
RN3 10K
RN4 10K
RN5 10K
RN6 10K
RN7 10K
RN8 10K
RN9 10K
RN10 10K
RN11 10K
RN12 10K
/RST
C7
J2
HDRD40
J1
H2
H3
H4
H1
HDRD2
J0
DJ-005
D2
1N5817
C16
10UF35V
STE
Title
P100
Size
B
Document Number
P100.SCH
REV
Date: October 29, 1999
Sheet 1 of 1


U1
U2
U3
U4
PPI8255
PPIS
SD107C65401
C1
C2
C3
C4
C6
C7
/RST
K
C18
10UF35V
X1
X2
10PF
C8
C9
20MHZ
XTAL2
U6
SJA1000
U7
MCP2551
R7
R6
C0
CANH
CANL
220
C17
H5
HDRD10
J3
J4
J5
J6
J7
J8
HDRD20
H8
H6
HDRS3
P32
/INT
P31
ALE1
ALE
ALE2
U9
LM2575
+12V
R5
1M
VOFF
LX1
D1
1N5817
I1
330 uH
RCH110
C01
C5
R2
R3
R1
RTS
CTS
220
10K
U10
LTC485
RXD
GND
MPO
TXD
U11
U12
MAX232A
C15
C14
C13
C12
C10
C11
U5
PAL16V8
P100CAN.PDS
H9
HDRS4
H7
H2
H4
H3
H1
HDRD10
HDRD2
J0
DJ-005
C16
J1
J2
HDRD40
RN1 10K
RN2 10K
RN3 10K
RN4 10K
RN5 10K
RN6 10K
RN7 10K
RN8 10K
RN9 10K
RN10 10K
RN11 10K
RN12 10K
U13
ULN2003
ULN2003A
TERN/STE
P100+CAN EXPANSION BOARD
Size B
Document Number P10C-MAN.SCH
REV
Date: March 25, 2008
Sheet 1 of 1