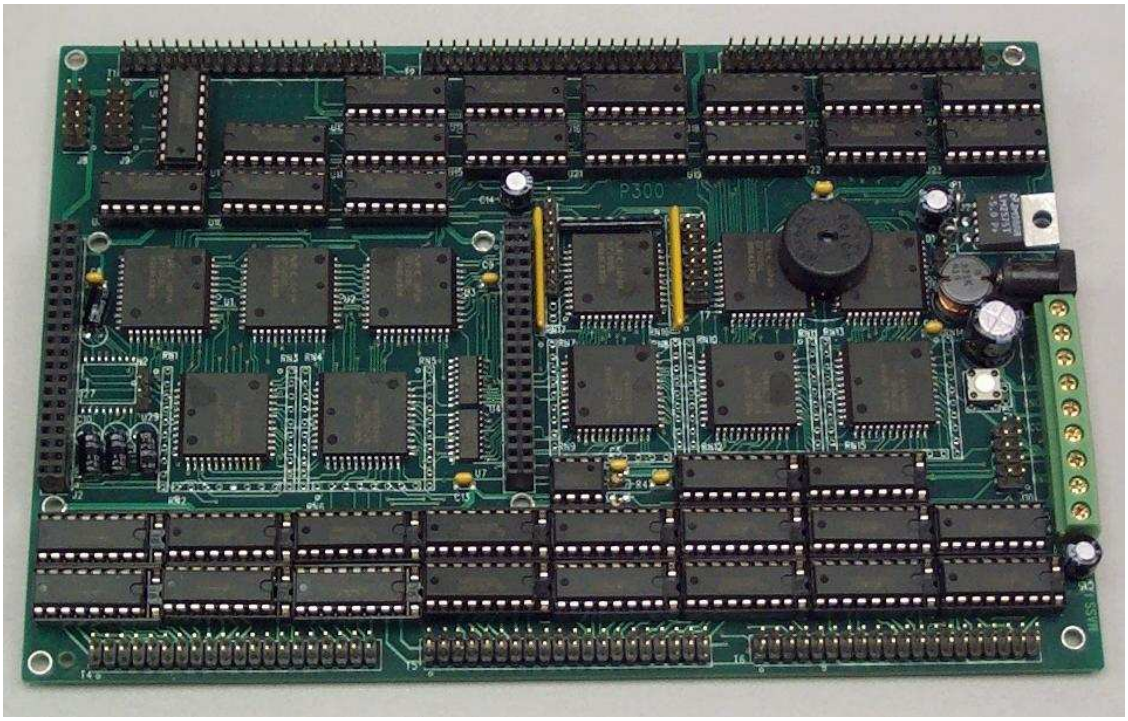
P300™

300+ I/Os, 240 solenoid drivers



Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

Measuring 7.5 x 5.0 x 0.5 inches, the ***P300*** offers a large I/O expansion to any TERN Engine board (A-Engine, A-Engine86, i386-Engine and R-Engine). The versatility of the ***P300*** allows the use of 240 TTL-level I/O, high voltage input and solenoid driving output plus LCD and keypad support. The ***P300*** is the perfect expansion board for applications where high speed and low cost are a concern.

The ***P300*** is designed for industrial control applications which require solenoid drivers and protected high-voltage inputs. There are 240 high-voltage I/O lines on the ***P300*** that can be configured as high voltage inputs or solenoid driving outputs. The inputs handle up to 35V DC. The outputs are capable of sinking 350 mA at 50V per line, and they can directly drive solenoids, relays, or lights. The high voltage chips may also be replaced with resistor pack ICs to provide digital TTL I/O to the user.

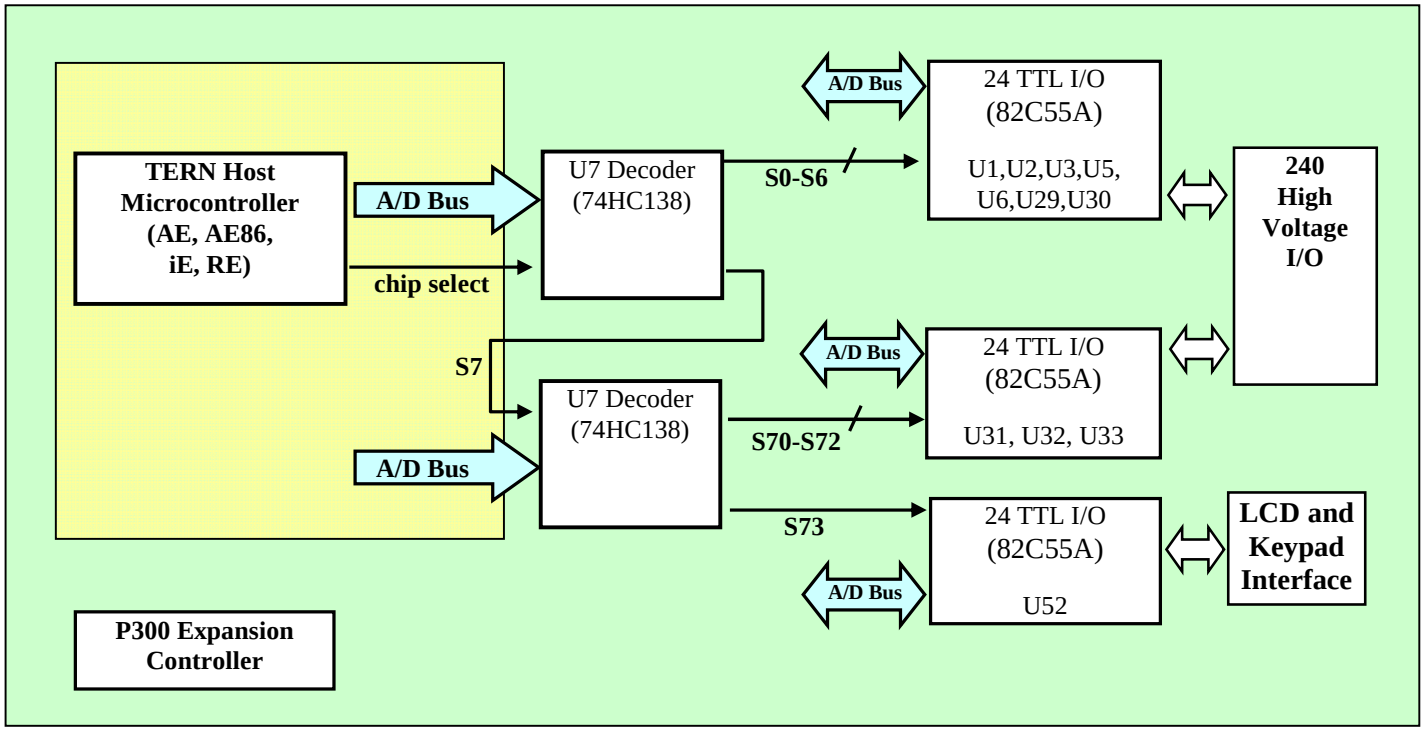


Figure 1.1 Functional block diagram of the P300

1.2 Features

Standard Features

- Dimensions: 7.5 x 5.0 x 0.5 inches
- Power input: +9V to +35 V unregulated DC (up to +35V with optional switching regulator)
- On-board +5V switching power supply
- On-board RS232/485 serial drivers
- 264 I/O pins supporting digital, high voltage, LCD/keypad interfacing

1.3 Physical Description

The physical layout of the P300 is shown in Figure 1.2.

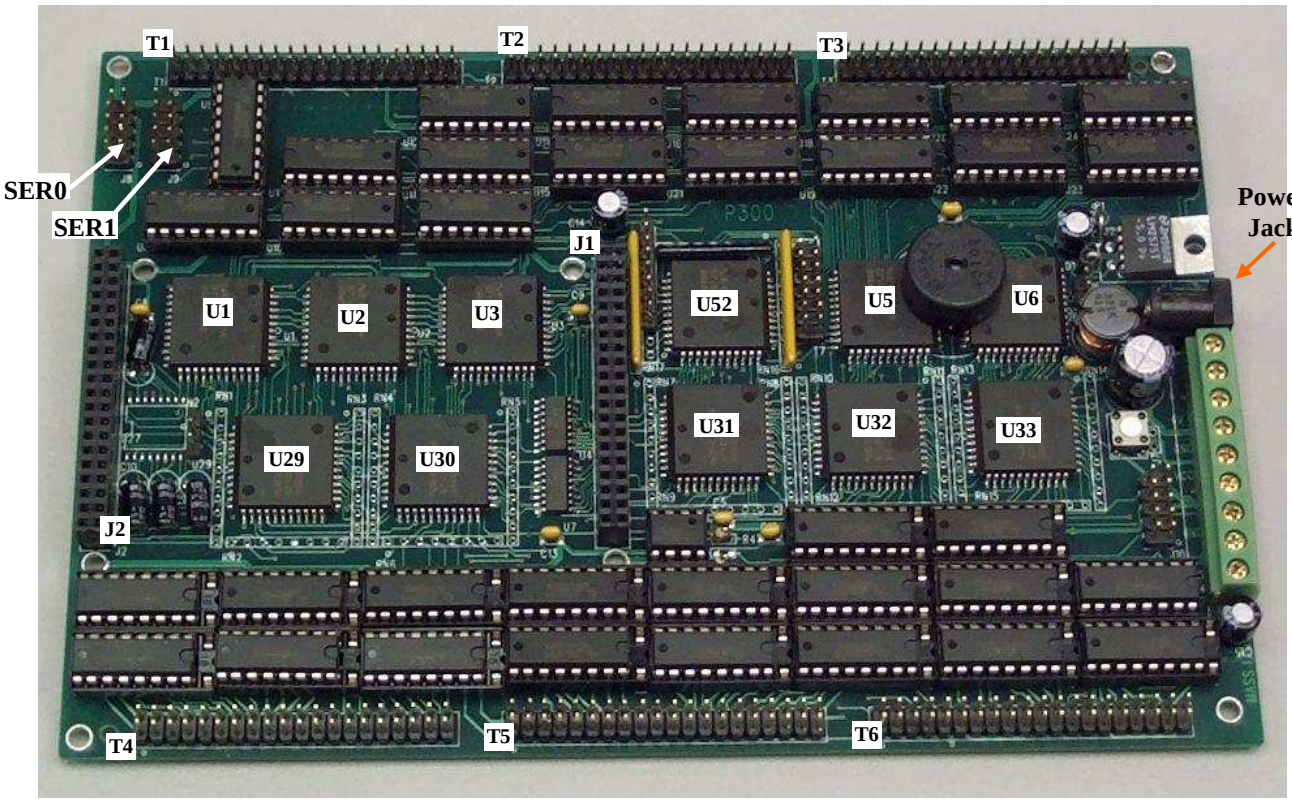


Figure 1.2 Physical layout of the P300

The physical layout/description of the P300 is shown above. Labels for pin headers are located nearest pin 1 of the respective header (also applies to the J1 and J2 expansion sockets). T4

Each 82C55A PPI chip is label by location and a letter which corresponds to a specific I/O address found in the p300.h header file (of the TERN host controller directory). For example, if the A-Engine is being used as the host controller, see **tern\186\include\p300.h**, and if using the i386-Engine, see **tern\386\include\p300.h**.

The table below will summarize the name of each 82C55A PPI chip.

Location	U1	U2	U3	U5	U6	U29	U30	U31	U32	U33	U52
Name	B	E	F	G	H	I	K	L	M	N	R

To find the I/O address for the U5 PPI chip, for example, open the appropriate header based on the host controller. If using the A-Engine, open **tern\186\include\p300.h**. Each PPI chip will have its own define statement based on its letter name. For U5, look for the '#define PPI**G** 0x2b0' statement.

1.4 Minimum Requirements for P300 System Development

1.4.1 Minimum Hardware Requirements

- PC or PC-compatible computer with serial COMx port that supports 115,200 baud
- TERN Engine controller (AE/AE86/iE/RE). See appropriate technical manual.
- Debug serial cable (RS232; DB9 connector for PC COM port and IDE 2x5 connector for controller)
- Center negative wall transformer (+9V 500 mA)

1.4.2 Minimum Software Requirements

- TERN EV-P/DV-P Kit CD-ROM
- PC software environment: Windows95/98/2000/ME/NT/XP

The C/C++ Evaluation Kit (EV-P) and C/C++ Development Kit (DV-P) are available from TERN. The EV-P Kit is a limited-functionality version of the DV-P Kit. With the EV-P Kit, the user can download and remote debug an application (STEP 1), as well as perform standalone field tests with the application residing in the battery-backed SRAM of the host controller (STEP 2). However, the DV-P Kit is required to generate application binary and HEX files for a final production version (STEP 3).

Chapter 2: Installation

2.1 Software Installation

The technical manual for the host controller will provide details about the software installation for evaluation of TERN controllers.

2.2 Hardware Installation

Hardware installation for the P300 consists of installing the host controller onto the P300 and connecting the P300 to power and the PC for remote debugging.

Overview

- Install the host controller onto the P300.
- Connect debug serial cable:
  For debugging (STEP 1), place IDE connector on SER0 (J8 pin header on the P300) with red edge of cable at pin 1.
- Connect wall transformer:
  Connect 9V wall transformer to power and plug into power jack

2.2.1 Installing the host controller onto the P300

Each host controller will install onto the P300 in the same manner. All that is necessary is to align the J1 and J2 pin headers on the host controller with the J1 and J2 expansion sockets on the P300. See the diagram below for illustrated details.

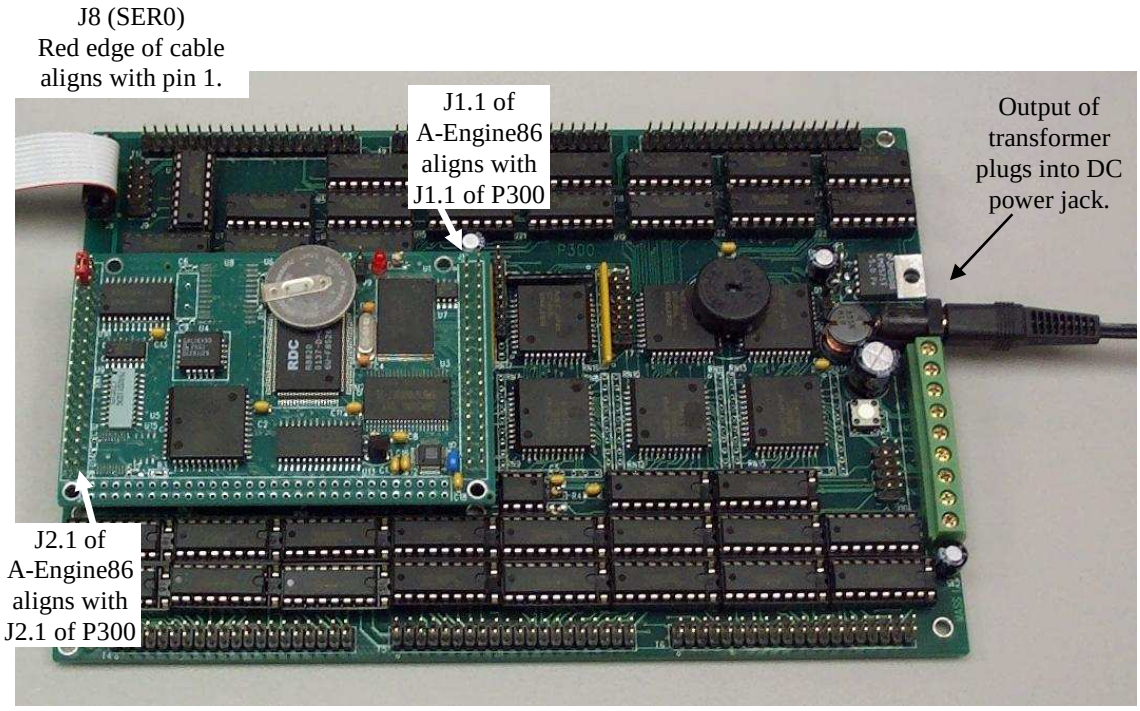
2.2.2 Connecting the P300 to the PC

The diagram below shows the link between the PC and the P300. It consists of connecting the debug serial cable to the PC and the SER0 pin header of the P300.

It is important to note the red edge of the 5x2 IDE connector must align with PIN 1 of the SER0 pin header. SER0 is located at J8 on the P300.

2.2.3 Powering-on the P300 & host controller

The TERN EV-P and DV-P Kits include a +9V DC power transformer. Plug the output of the transformer into the DC power jack on the P300. Refer to the following diagram. Upon power-up, the on-board LED of the host controller should blink twice and remain on to indicate ready for remote debugging.



A-Engine86 installed onto the P300; connected to PC via serial debug cable and output of transformer.

Chapter 3: Hardware

3.1 Engine controllers

The P300 must be driven by an "Engine controller", such as the A-Engine, A-Engine86, i386-Engine, or R-Engine. The "Engine" installs on top of the P300 via the 20x2 pin headers J1 and J2, and can be secured by two #4-40 mounting screws. See Chapter 2 for full installation details.

3.2 Serial Ports Drivers

The P300 can provide up to 3 channels RS-232/485 drivers. Two RS-232 drivers are installed to interface the two asynchronous serial channels from the installed Engine controller via 20x2 pin header J1 and J2. In addition, the Engine controller can support an additional UART. The P300 can be configured to interface the additional UART with an RS-232 or RS-458 driver.

The default debug serial port, SER0, is routed to J8, SER1 is at J9, and the SCC port is at J10. Part specifications for the serial port drivers can be found in the tern_docs\parts directory of the TERN installation CD (max232.pdf and sn75lbc184.pdf).

3.3 I/O Mapped Devices

3.3.1 I/O Space

External I/O devices use I/O mapping for access. You can access such I/O devices with ***inportb(port)*** or ***outportb(port,dat).*** These functions will transfer one byte of data to/from the specified I/O address. Each PPI (82c55a) device is identified by a letter. Each letter then corresponds to its matching I/O address, which can be found in p300.h of the host controller's directory. Chapter 1 of this manual gives a table and diagram for identifying each PP1.

3.3.2 Programmable Peripheral Interface (82C55A)

The PPI (82C55, or uPD81055L) is a low-power CMOS programmable parallel interface unit for use in microcomputer systems. They each provide 24 TTL level I/O pins that may be individually programmed in two groups of 12 and used in three major modes of operation. Eleven are installed on the P300 for a total of 264 I/Os. They are found in locations U1, U2, U3, U5, U6, U29, U30, U32, U32, U33, and U52.

In MODE 0, two groups of 12 pins can be programmed in sets of 4 and 8 pins to be inputs or outputs. In MODE 1, each of the two groups of 12 pins can be programmed to have 8 lines of input or output. Of the 4 remaining pins, 3 are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

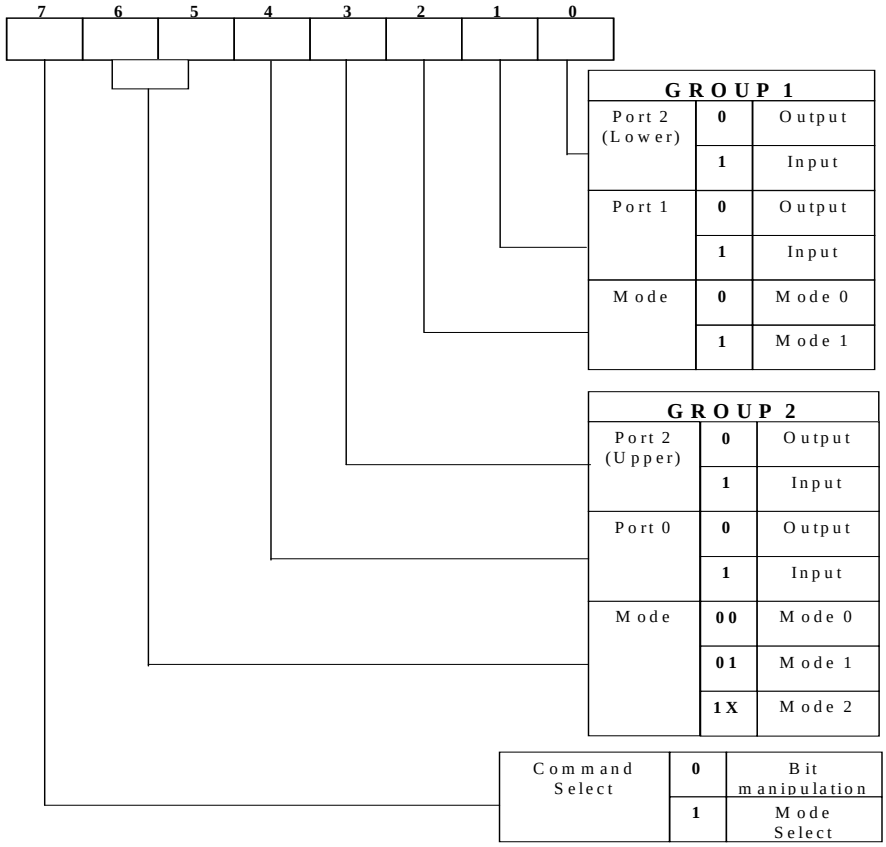


Figure 3.1 Mode Select Command Word

To program the PPI, determine the necessary command word based on chart above. This value must be written to the PPI's command register. For an example, consider the PPI at location U1. The P300 maps U1, the PPIU**B** 82C55/uPD71055, at base I/O address PPIUB = 0x??80. The ?? address will vary based on host controller. Here, the registers will map as follows:

Command Register = PPIUB+3
Port 0 = PPIUB
Port 1 = PPIUB+1
Port 2 = PPIUB+2

Two possible configurations will be shown.

(1) Set all ports to output mode (Mode 0)

```
outportb(PPIUB+3,0x80);
```

The output pins can then be driven by writing to each port:

```
outportb(PPIUB+0,0x55);
outportb(PPIUB+1,0x55);
outportb(PPIUB+2,0x55);
```

(2) Set all ports to input mode:

```
outportb(PPIUB+3,0x9f);
```

The input ports can be read using one inport statement per port:

```
inportb(PPIUB+0); /* Port 0 */
inportb(PPIUB+1); /* Port 1 */
inportb(PPIUB+2); /* Port 2 */
```

This returns an 8-bit value for each port, with each bit corresponding to the appropriate line on the port.

There are a total of 24x11 TTL level I/O pins, all free for applications use. These I/O lines are specified as 4 mA driving current capability. The PPI at location U52 is located near the center of the P300. Its I/Os are routed directly to headers T7 and T8. Each port is pulled-up via 10K resistor for easy implementation of an LCD/keypad interface. (Refer to sample code p300_kp.c)

Refer to the P300 schematics at the end of this manual (or tern_docs\schs) for additional pin location details. The data sheet for the 82C55A can be found in the tern_docs\parts directory under "82c55a.pdf".

3.4 High-Voltage, High-Current Drivers

The ULN2003 has high voltage, high current Darlington transistor arrays, consisting of 7 silicon NPN Darlington pairs on a common monolithic substrate. All channels feature open-collector outputs for sinking 350 mA at 50V, and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA sinking are allowed. These outputs may be paralleled to achieve high-load capability, although each driver has a maximum continuous collector current rating of 350 mA at 50V. The maximum power dissipation allowed is 2.20 W per chip at 25 degree C. The common substrate, G, is routed to GND. All currents sinking in must return to GND. A heavy gage (20) wire must be used to connect GND to an external common ground return. K connects to the protection diodes in the ULN2003 chips and should be tied to highest voltage in the external load system. K can be connected to an unregulated on board +12V. **ULN2003 is a sinking driver not sourcing driver.** Typical application wiring is shown below.

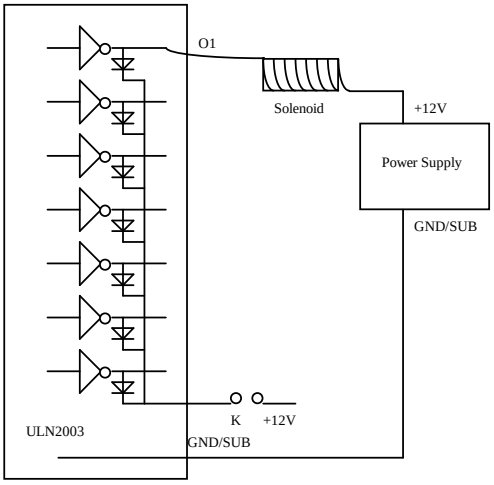


Figure 3.2 Drive inductive load with high voltage/current drives.

The P300 uses 35 ULN2003 devices, providing one high voltage channel per 240 TTL level I/O. By default all channels are high voltage output. Other possible configurations include replacing the ULN2003s with IC resistor packs for TTL level I/O. See the ULN2003 data sheet, "uln2003a.pdf", found in the tern_docs\parts directory on the TERN installation CD for additional details.

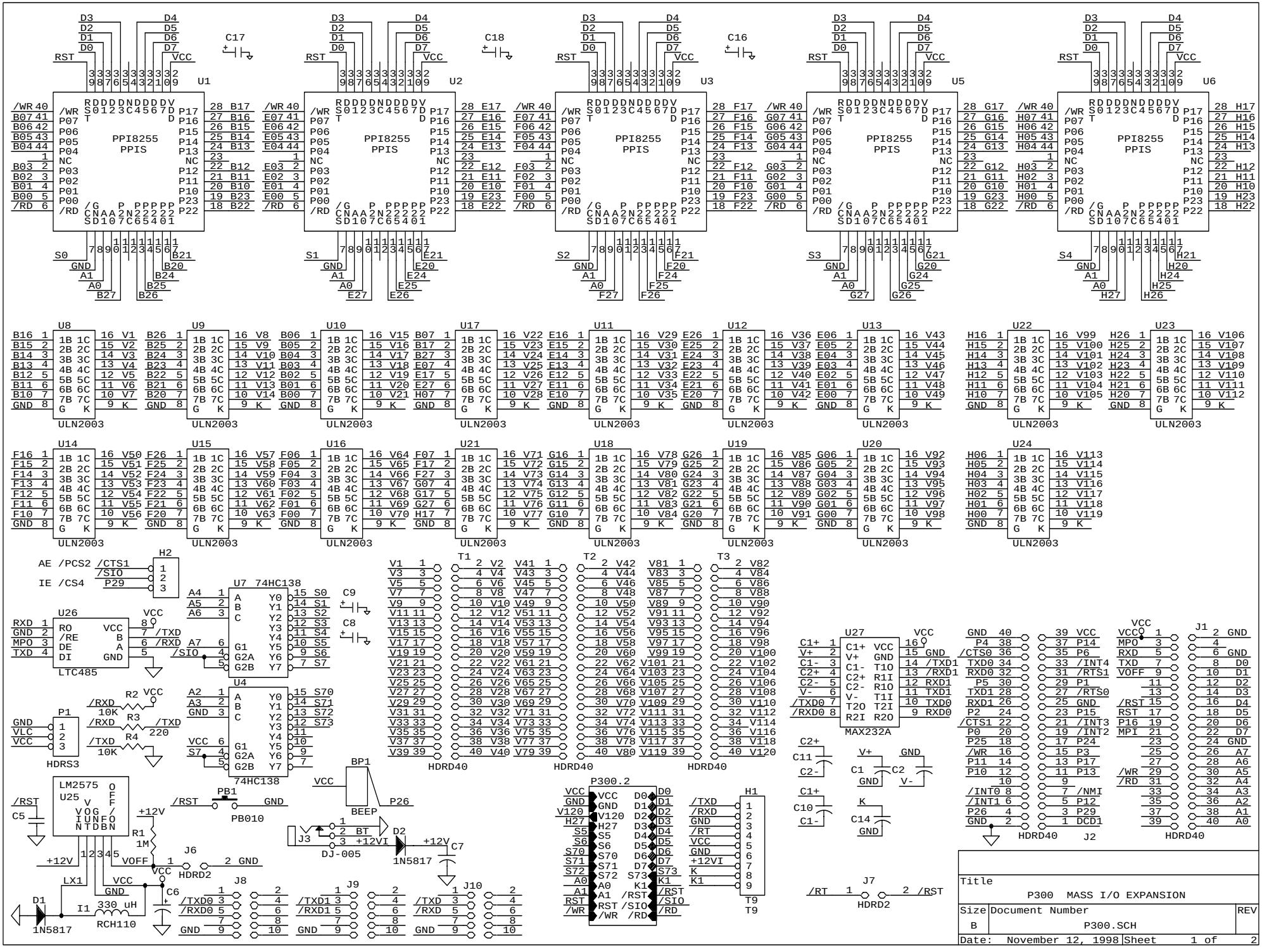
Appendix A: Board Modification

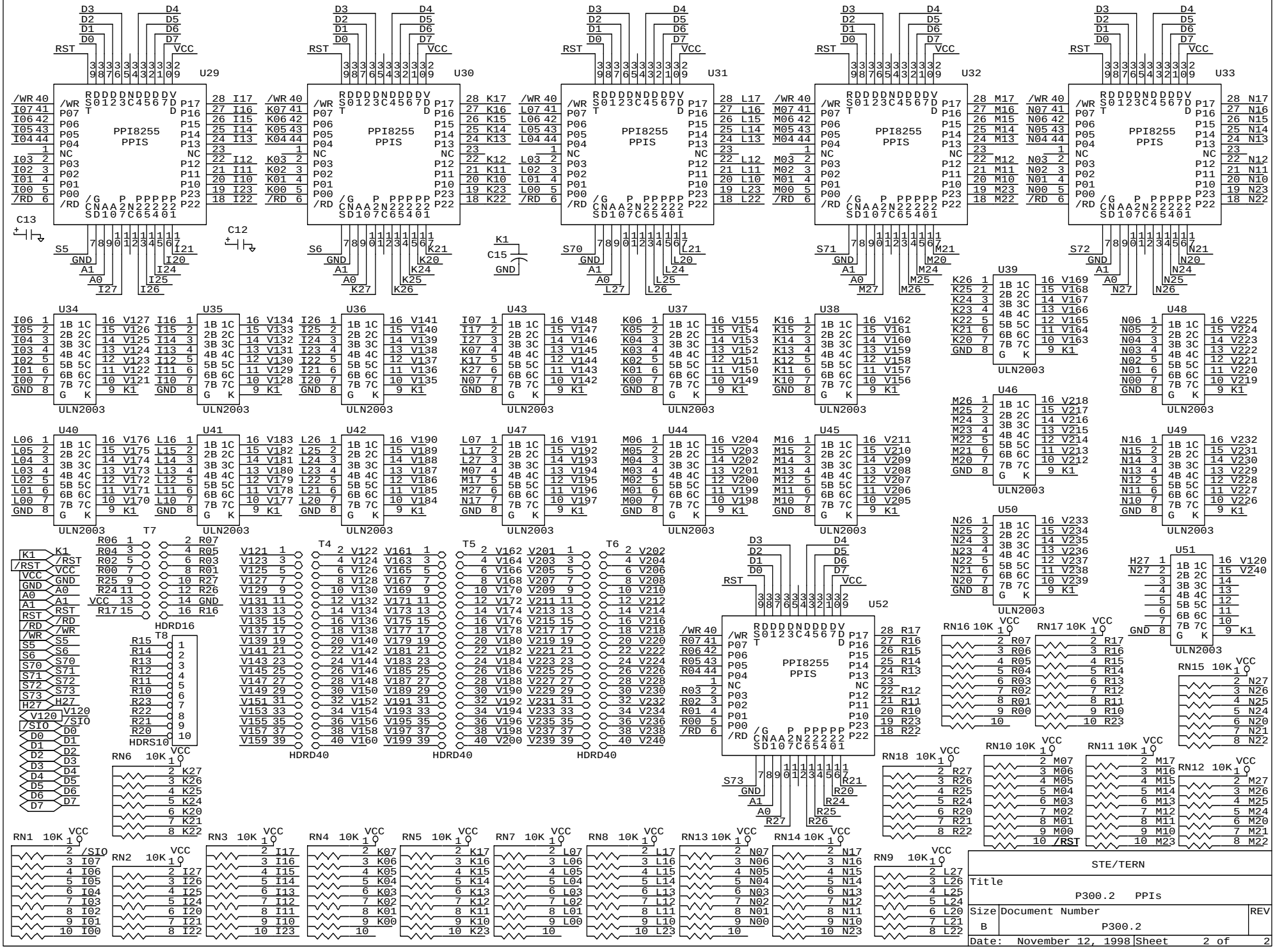
P300™ modifications to support VE, AE, AE86, RE, 386E, 586E 01-05-2005

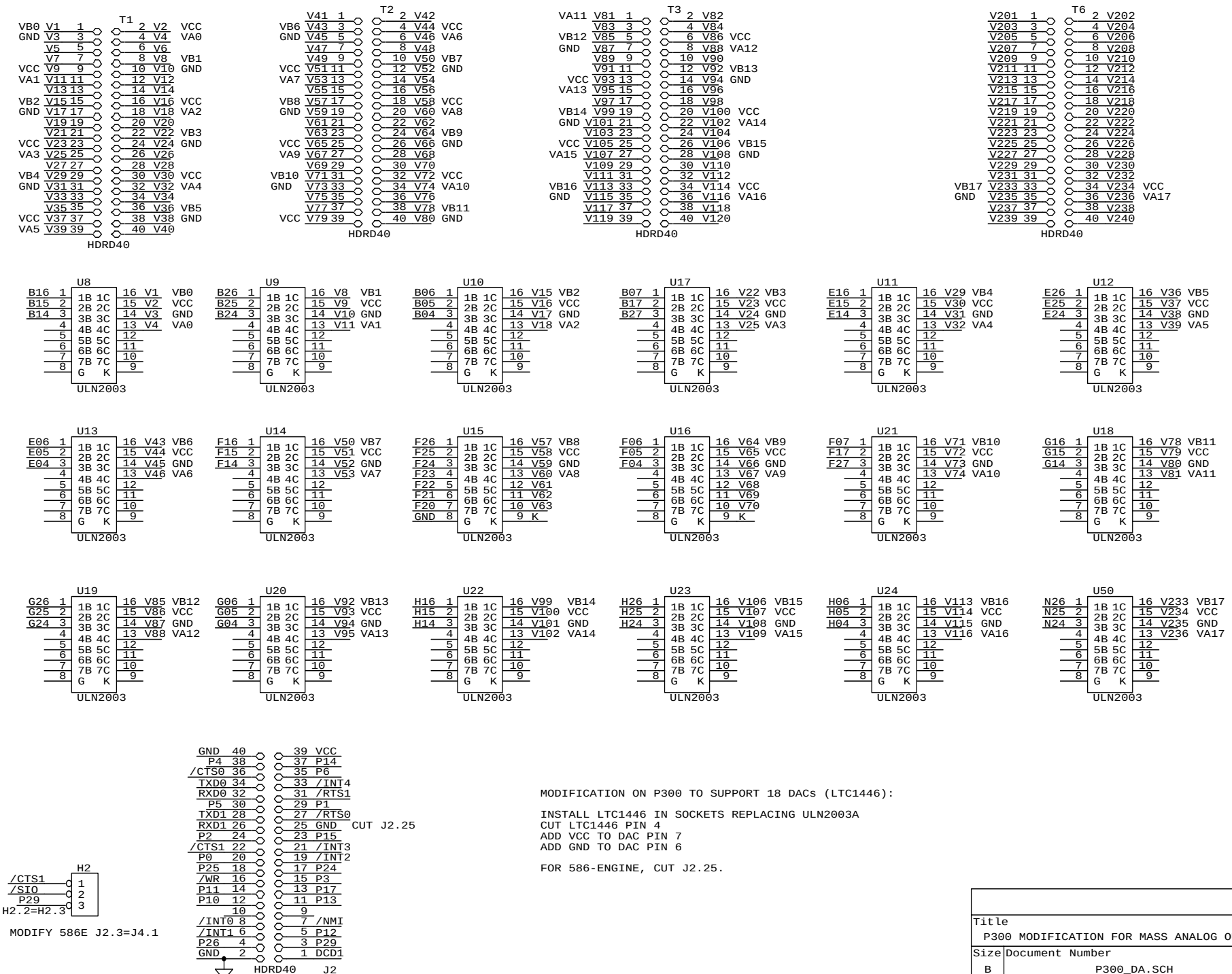
P300 was designed for V25-Engine in 1994.
P300 J2 header signals NOT compatible to all “Engines” are J2.25=GND, J2.16=/WR, J2.22=/CTS1.
P300 H2 provides selection for I/O select line /SIO: H2.1=J2.22, H2.2=/SIO, H2.3=J2.3

Modification needs to cut pins on J2.25, J2.16, no connection between P300 and Engine controller.

For RE:
1) Add wire connect J2.22=J2.31 to use P19=/PCS3
2) Jumper on P300 H1.1=H1.2=J2.2=J2.31 to use P19=/PCS3
3) Cut pins on J2.25, J2.16, no connection between P300 and RE
J2 pin 16 = /WR must be cut off the pin on “Engine” or cut off the trace on P300 PCB.


U1
U2
U3
U5
U6
PPI8255
PPIS
C17
C18
C16
U8
U9
U10
U17
U11
U12
U13
U22
U23
ULN2003
U14
U15
U16
U21
U18
U19
U20
U24
H2
U7 74HC138
U4 74HC138
C9
C8
U26
LTC485
P1
HDRS3
R2
R3
R4
10K
220
U27
MAX232A
C11
C1
C2
C10
C14
J1
J2
T1
T2
T3
HDRD40
P300.2
H1
T9
J7
HDRD2
BP1
BEEP
PB1
PB010
J3
DJ-005
D2
1N5817
C7
U25
LM2575
C5
R1
1M
J6
J8
J9
J10
LX1
C6
D1
I1
330 uH
RCH110
Title
P300 MASS I/O EXPANSION
Size
B
Document Number
P300.SCH
REV
Date: November 12, 1998
Sheet 1 of 2


U29
U30
U31
U32
U33
PPI8255
PPIS
U34
U35
U36
U43
U37
U38
U39
U48
U46
U49
U40
U41
U42
U47
U44
U45
U50
U51
U52
ULN2003
HDRD16
HDRS10
HDRD40
T4
T5
T6
T7
T8
RN1 10K
RN2 10K
RN3 10K
RN4 10K
RN5 10K
RN6 10K
RN7 10K
RN8 10K
RN9 10K
RN10 10K
RN11 10K
RN12 10K
RN13 10K
RN14 10K
RN15 10K
RN16 10K
RN17 10K
RN18 10K
C13
C12
C15
K1
VCC
GND
STE/TERN
Title
P300.2 PPIs
Size B
Document Number P300.2
REV
Date: November 12, 1998
Sheet 2 of 2


T1
VB0 V1 1 2 V2 VCC
GND V3 3 4 V4 VA0
V5 5 6 V6
V7 7 8 V8 VB1
VCC V9 9 10 V10 GND
VA1 V11 11 12 V12
V13 13 14 V14
VB2 V15 15 16 V16 VCC
GND V17 17 18 V18 VA2
V19 19 20 V20
V21 21 22 V22 VB3
VCC V23 23 24 V24 GND
VA3 V25 25 26 V26
V27 27 28 V28
VB4 V29 29 30 V30 VCC
GND V31 31 32 V32 VA4
V33 33 34 V34
V35 35 36 V36 VB5
VCC V37 37 38 V38 GND
VA5 V39 39 40 V40
HDRD40
T2
V41 1 2 V42
VB6 V43 3 4 V44 VCC
GND V45 5 6 V46 VA6
V47 7 8 V48
V49 9 10 V50 VB7
VCC V51 11 12 V52 GND
VA7 V53 13 14 V54
V55 15 16 V56
VB8 V57 17 18 V58 VCC
GND V59 19 20 V60 VA8
V61 21 22 V62
V63 23 24 V64 VB9
VCC V65 25 26 V66 GND
VA9 V67 27 28 V68
V69 29 30 V70
VB10 V71 31 32 V72 VCC
GND V73 33 34 V74 VA10
V75 35 36 V76
V77 37 38 V78 VB11
VCC V79 39 40 V80 GND
HDRD40
T3
VA11 V81 1 2 V82
V83 3 4 V84
VB12 V85 5 6 V86 VCC
GND V87 7 8 V88 VA12
V89 9 10 V90
V91 11 12 V92 VB13
VCC V93 13 14 V94 GND
VA13 V95 15 16 V96
V97 17 18 V98
VB14 V99 19 20 V100 VCC
GND V101 21 22 V102 VA14
V103 23 24 V104
VCC V105 25 26 V106 VB15
VA15 V107 27 28 V108 GND
V109 29 30 V110
V111 31 32 V112
VB16 V113 33 34 V114 VCC
GND V115 35 36 V116 VA16
V117 37 38 V118
V119 39 40 V120
HDRD40
T6
V201 1 2 V202
V203 3 4 V204
V205 5 6 V206
V207 7 8 V208
V209 9 10 V210
V211 11 12 V212
V213 13 14 V214
V215 15 16 V216
V217 17 18 V218
V219 19 20 V220
V221 21 22 V222
V223 23 24 V224
V225 25 26 V226
V227 27 28 V228
V229 29 30 V230
V231 31 32 V232
VB17 V233 33 34 V234 VCC
GND V235 35 36 V236 VA17
V237 37 38 V238
V239 39 40 V240
HDRD40
U8
B16 1 1B 1C 16 V1 VB0
B15 2 2B 2C 15 V2 VCC
B14 3 3B 3C 14 V3 GND
4 4B 4C 13 V4 VA0
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U9
B26 1 1B 1C 16 V8 VB1
B25 2 2B 2C 15 V9 VCC
B24 3 3B 3C 14 V10 GND
4 4B 4C 13 V11 VA1
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U10
B06 1 1B 1C 16 V15 VB2
B05 2 2B 2C 15 V16 VCC
B04 3 3B 3C 14 V17 GND
4 4B 4C 13 V18 VA2
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U17
B07 1 1B 1C 16 V22 VB3
B17 2 2B 2C 15 V23 VCC
B27 3 3B 3C 14 V24 GND
4 4B 4C 13 V25 VA3
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U11
E16 1 1B 1C 16 V29 VB4
E15 2 2B 2C 15 V30 VCC
E14 3 3B 3C 14 V31 GND
4 4B 4C 13 V32 VA4
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U12
E26 1 1B 1C 16 V36 VB5
E25 2 2B 2C 15 V37 VCC
E24 3 3B 3C 14 V38 GND
4 4B 4C 13 V39 VA5
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U13
E06 1 1B 1C 16 V43 VB6
E05 2 2B 2C 15 V44 VCC
E04 3 3B 3C 14 V45 GND
4 4B 4C 13 V46 VA6
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U14
F16 1 1B 1C 16 V50 VB7
F15 2 2B 2C 15 V51 VCC
F14 3 3B 3C 14 V52 GND
4 4B 4C 13 V53 VA7
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U15
F26 1 1B 1C 16 V57 VB8
F25 2 2B 2C 15 V58 VCC
F24 3 3B 3C 14 V59 GND
F23 4 4B 4C 13 V60 VA8
F22 5 5B 5C 12 V61
F21 6 6B 6C 11 V62
F20 7 7B 7C 10 V63
GND 8 G K 9 K
ULN2003
U16
F06 1 1B 1C 16 V64 VB9
F05 2 2B 2C 15 V65 VCC
F04 3 3B 3C 14 V66 GND
4 4B 4C 13 V67 VA9
5 5B 5C 12 V68
6 6B 6C 11 V69
7 7B 7C 10 V70
8 G K 9 K
ULN2003
U21
F07 1 1B 1C 16 V71 VB10
F17 2 2B 2C 15 V72 VCC
F27 3 3B 3C 14 V73 GND
4 4B 4C 13 V74 VA10
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U18
G16 1 1B 1C 16 V78 VB11
G15 2 2B 2C 15 V79 VCC
G14 3 3B 3C 14 V80 GND
4 4B 4C 13 V81 VA11
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U19
G26 1 1B 1C 16 V85 VB12
G25 2 2B 2C 15 V86 VCC
G24 3 3B 3C 14 V87 GND
4 4B 4C 13 V88 VA12
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U20
G06 1 1B 1C 16 V92 VB13
G05 2 2B 2C 15 V93 VCC
G04 3 3B 3C 14 V94 GND
4 4B 4C 13 V95 VA13
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U22
H16 1 1B 1C 16 V99 VB14
H15 2 2B 2C 15 V100 VCC
H14 3 3B 3C 14 V101 GND
4 4B 4C 13 V102 VA14
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U23
H26 1 1B 1C 16 V106 VB15
H25 2 2B 2C 15 V107 VCC
H24 3 3B 3C 14 V108 GND
4 4B 4C 13 V109 VA15
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U24
H06 1 1B 1C 16 V113 VB16
H05 2 2B 2C 15 V114 VCC
H04 3 3B 3C 14 V115 GND
4 4B 4C 13 V116 VA16
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
U50
N26 1 1B 1C 16 V233 VB17
N25 2 2B 2C 15 V234 VCC
N24 3 3B 3C 14 V235 GND
4 4B 4C 13 V236 VA17
5 5B 5C 12
6 6B 6C 11
7 7B 7C 10
8 G K 9
ULN2003
H2
/CTS1 1
/SIO 2
P29 3
586 H2.2=H2.3
MODIFY 586E J2.3=J4.1
GND 40 39 VCC
P4 38 37 P14
/CTS0 36 35 P6
TXD0 34 33 /INT4
RXD0 32 31 /RTS1
P5 30 29 P1
TXD1 28 27 /RTS0
RXD1 26 25 GND CUT J2.25
P2 24 23 P15
/CTS1 22 21 /INT3
P0 20 19 /INT2
P25 18 17 P24
/WR 16 15 P3
P11 14 13 P17
P10 12 11 P13
10 9
/INT0 8 7 /NMI
/INT1 6 5 P12
P26 4 3 P29
GND 2 1 DCD1
HDRD40 J2
MODIFICATION ON P300 TO SUPPORT 18 DACs (LTC1446):
INSTALL LTC1446 IN SOCKETS REPLACING ULN2003A
CUT LTC1446 PIN 4
ADD VCC TO DAC PIN 7
ADD GND TO DAC PIN 6
FOR 586-ENGINE, CUT J2.25.
Title
P300 MODIFICATION FOR MASS ANALOG OUTPUTS
Size B
Document Number P300_DA.SCH
REV
Date: September 29, 2003
Sheet 1 of 2