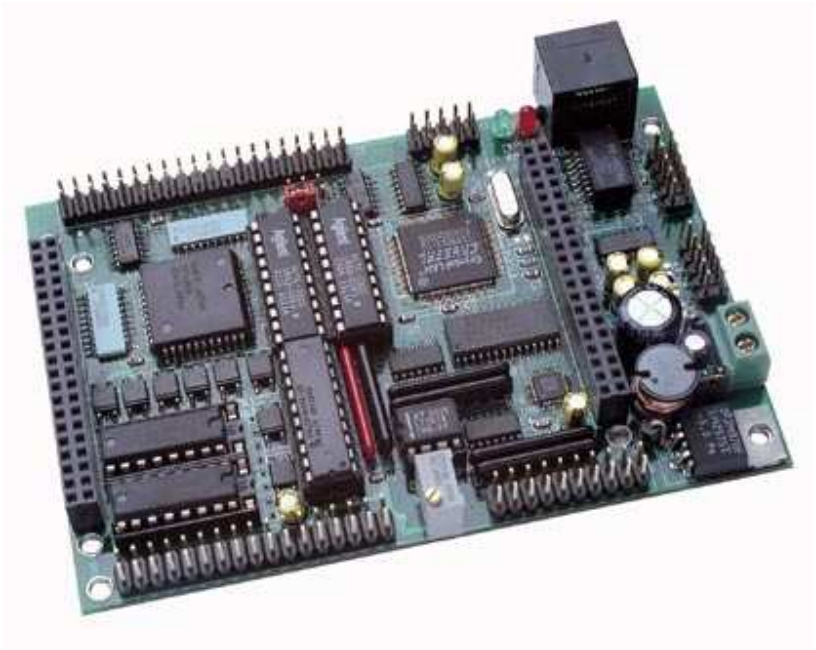
P50™

I/O expansion card with ADC, DAC, 24 PPI I/Os, 10-BaseT Ethernet, Quadrature Decoders, RS232/485



Technical Manual

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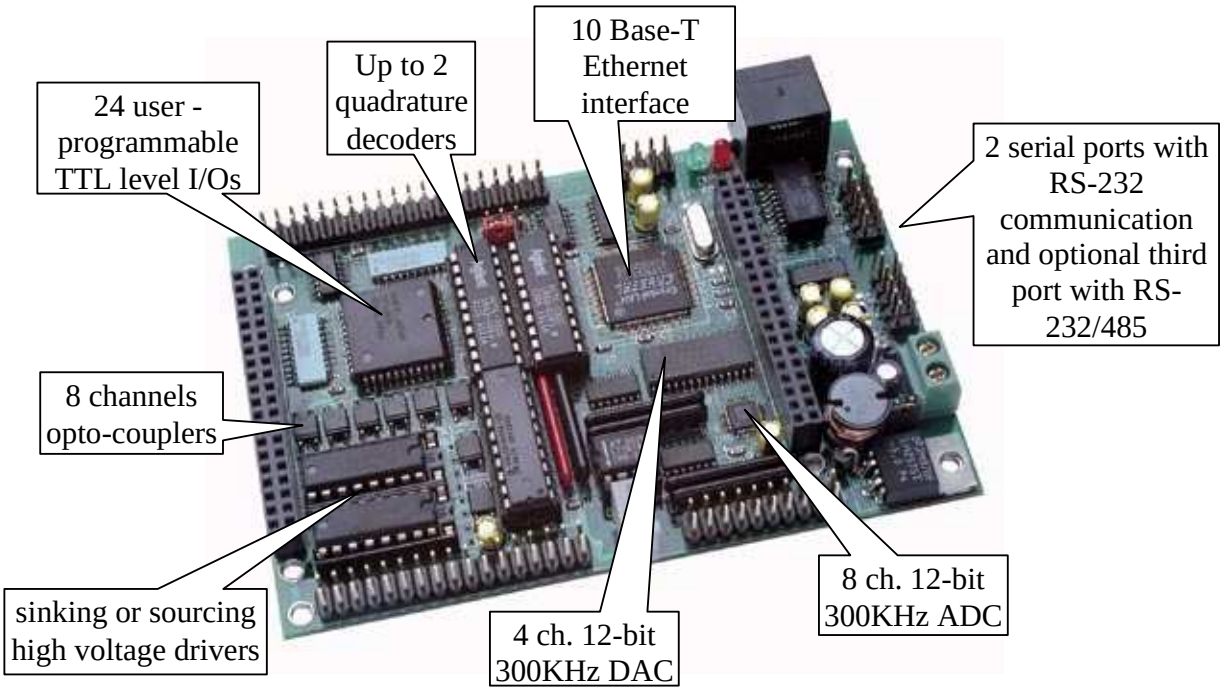
Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

Measuring 4.4 x 3.1 inches, the ***P50™*** is an I/O expansion board designed for and driven by a 586-Engine™. A 16-bit external data bus is required to run the parallel ADC and DAC on the P50. Many embedded applications demand high speed ADC and DAC with buffered operational amplifiers supporting variable gains or offset for analog signals. The P50 supports four 12-bit, 300KHz, parallel DACs (DAC7625, 2.5V) buffered by 4 ops with gain=2 (hardware adjustable), providing 0-5V analog output by default. It also supports eight 12-bit 300KHz parallel ADC (ADS7852, 0-5V) with four inputs buffered by 4 ops. A precision voltage reference (LT1019) with build-in temperature sensor can be installed. A resistor pot is used to adjust the DAC analog output offset.

The 586-Engine has 32 0-3.3V PIOs on the J2 header. The P50 can buffer PIOs with 16 sourcing drivers (UDN2982), or 14 sinking drivers (ULN2003). These drivers can source or sink 350 mA at 50V per line to directly drive solenoids, relays, or lights. Seven high voltage drivers can be re-configured as high voltage inputs. Eight high isolation voltage photocouplers (PS2701, NEC) can be installed to provide optically isolators to PIOs. Two quadrature decoders, (HCTL2020, Hewlett Packard) can be installed to interface incremental motion encoders. In addition, 24 bi-directional TTL PPI I/Os (82C55) are software programmable and free to use.



An Ethernet LAN controller (CS8900) can be installed to provide network connectivity. A RJ45 8-pin connector is used to connect to a 10-baseT Ethernet network. A software stack library is available, supporting network protocols like ARP, DHCP, UDP, ICMP, and of course TCP over the Ethernet network.

Two channels of RS-232 drivers and a 5V linear regulator are on-board. An optional RS232 or RS485 driver can be installed for the optional 3rd UART of the 586-Engine. The ***P50*** requires 8.5V to 12V DC

power supply with linear regulator, or up to 30V DC power input with an optional switching regulator without generating excessive heat.

An i386-Engine, or a A-Engine86 can be installed on the P50 with limitations, lacking proper PIO lines on the J2 header. Only 8 high voltage drivers and 5 opto-couplers are available for the A-Engine86. Only 9 high voltage drivers and 8 opto-couplers are available for the i386-Engine.

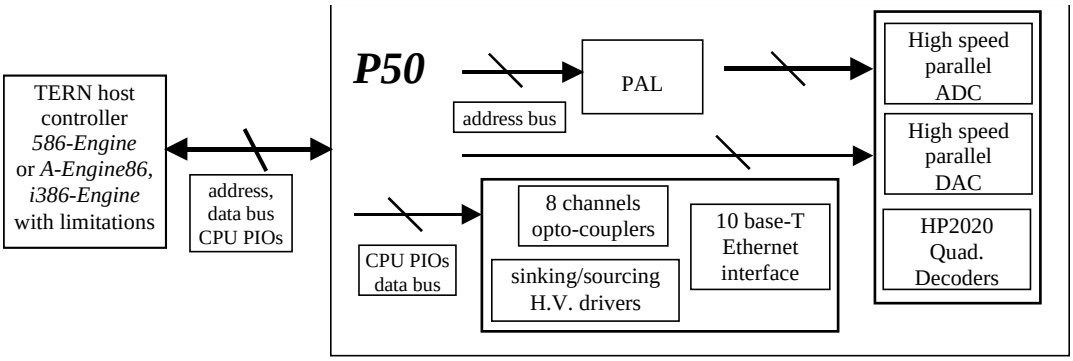


Figure 1.1 Functional block diagram of the P50

1.2 Features

► 4.4x3.1x0.5 inches.
► Driven by ***586-Engine™*** , ***i386-Engine™, A-Engine86™***.
► Power consumption: < 200 mA @ 9V-12V
► 2 channels RS-232 serial communication
► 24 PPIs, 14 high voltage sourcing or sinking drivers
► CS8900 10 Base-T Ethernet Controller*.
► 8 ch. 12-bit 300KHz ADC(ADS7852) with 4 input ops*.
► 4 ch. 12-bit 300KHz DAC(DAC7625) with buffer ops*.
► 8 opto-isolators and 2 quadrature decoders*
► 5V switching regulator*
► RS-232/485 for optional 3rd UART on controlling 'Engine'*
*optional

Chapter 2: Installation

2.1.1 Connecting the P50 and the 586-Engine to the PC

The following diagram (Figure 2.1) illustrates the connection between the P50 and the PC via a serial cable.

A 586-Engine controller must be installed on the P50 via J1 and J2 headers ***before power on***. The 586-Engine communicates through SER0 for debugging by default. Thus, the 5x2 IDC connector must be installed on the SER0 of the P50 (header H2). ***IMPORTANT:*** *Note that the* ***red*** *side of the cable must point to pin 1 of the H2 header.* The DB9 connector should be connected to one of your PC's COM Ports (COM1 or COM2).

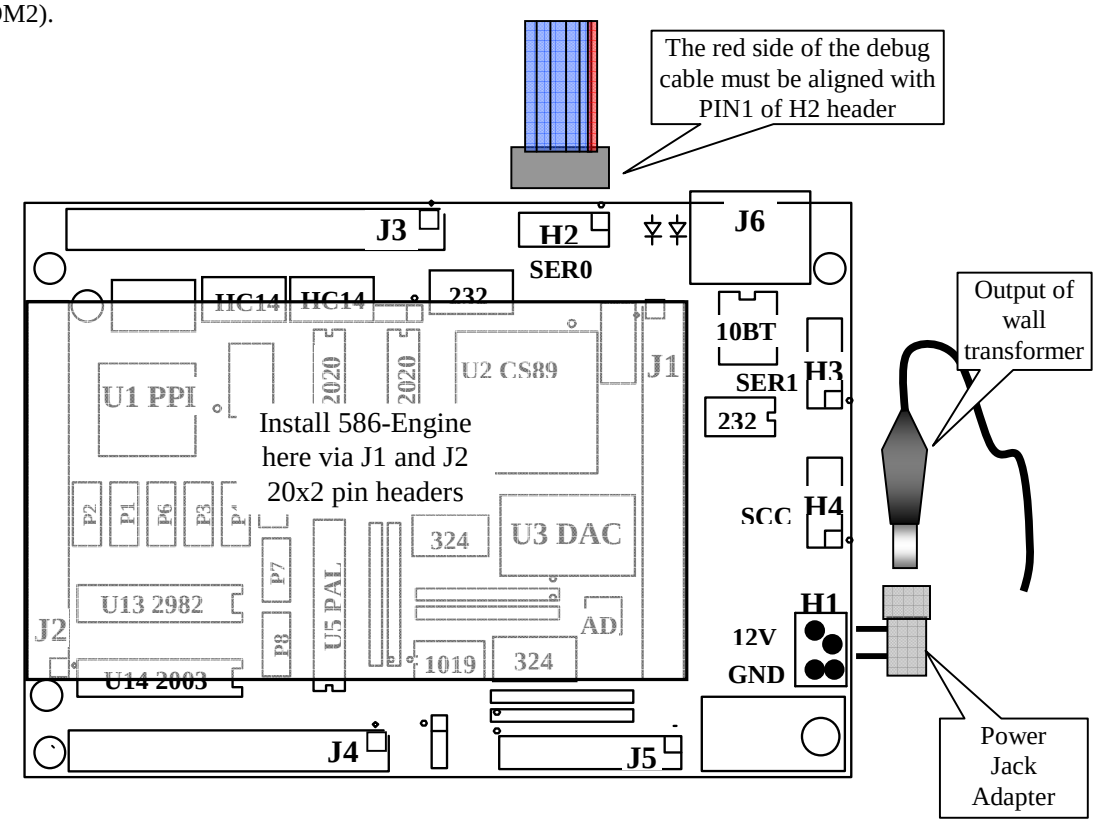


Figure 2.1 The P50 mounted to host 586-Engine via J1, J2 with the P50 connected to PC via debug cable

The P50 must be powered by an unregulated +12 Volts (or up to +30V with an optional switching regulator). A 2x1 screw terminal is installed to accept this +12V input. See schematic for orientation of screw terminal. Using the power jack adapter provided with a TERN EV-P or DV-P Kit, connect the output of the wall transformer to your P50 (as seen in above diagram).

Chapter 3: Hardware

3.1 Engine controllers

The P50 was designed to be driven by the 586-Engine, using the 16-bit external data/address bus to drive the parallel ADC and DAC, while at the same time using CPU PIOs to drive the high voltage drivers and opto-couplers. The P50 can also be driven by other 'Engine' controllers, such as the A-Engine86 or i386-Engine, but with limited functionality. Both the AE86 and the IE wil support the 12-bit ADC and DAC, yet do not provide the same amount of CPU PIOs for other components like the high voltage drivers, or the opto-couplers. Any 'Engine' used will installed on top of the P50 via 20x2 pin headers J1 and J2, and can be secured by two #4-40 mounting screws.

3.2 Serial Ports Drivers

The P50 can provide up to 3 channels RS-232/485 drivers. By default, two RS-232 drivers are ready for the two asynchronous serial UARTs from the installed Engine controller via 20x2 pin header J1 and J2. One optional 3rd RS232 or RS485 driver can be installed to support the optional UART SCC2691 on the Engine controller.

The default debug serial port SER0 is routed at H2, SER1 at H3, and SCC port at H4.

3.3 I/O Mapped Devices

3.3.1 I/O Space

External I/O devices can use I/O mapping for access. You can access such I/O devices with ***inportb(port)*** or ***outportb(port,dat)***. These functions will transfer one byte of data to the specified I/O address. Refer to the software chapter of the controlling Engine's technical manual for additional information on I/O space and access.

The table below shows more information about I/O mapping,

For the 586-Engine, selected by P27=/GPCS0=J2.37:

I/O space	Select Signal	Location	Usage
0x1800-0x1803	/PP1	U1 pin 7	/PPI for PPI
0x1810	/AD	U15 pin 31	/ADC for ADS7852
0x1820 /WR	/DA	U3 pin 23	/DA for 12-bit DAC7625
0x1820 /RD	/HP1	U6 pin 4	read HP2020 (U6)
0x1830	/HP2	U8 pin 4	read HP2020(U8)
0x1840	/CS89	U2 pin 63	/CS8900 Ethernet controller

NOTE: Although set at the factory, before shipping, the P50 pin header H7 must have the correct jumper set based on the driving 'Engine'. For the 586-Engine, set H7.1=H7.2 on the P50, while for the A-Engine86 and i386-Engine, set H7.2=H7.3 on the P50. This routes the correct chip select line of the 'Engine' to the PAL on the P50 to correctly select I/O peripherals.

3.3.2 Programmable Peripheral Interface (82C55A)

The U1 PPI (8255) is a low-power CMOS programmable parallel interface unit for use in microcomputer systems. It provides 24 I/O pins that may be individually programmed in two groups of 12 and used in three major modes of operation.

In MODE 0, the two groups of 12 pins can be programmed in sets of 4 and 8 pins to be inputs or outputs. In MODE 1, each of the two groups of 12 pins can be programmed to have 8 lines of input or output. Of the 4 remaining pins, 3 are used for handshaking and interrupt control signals. Finally, MODE 2 is a strobed bi-directional bus configuration.

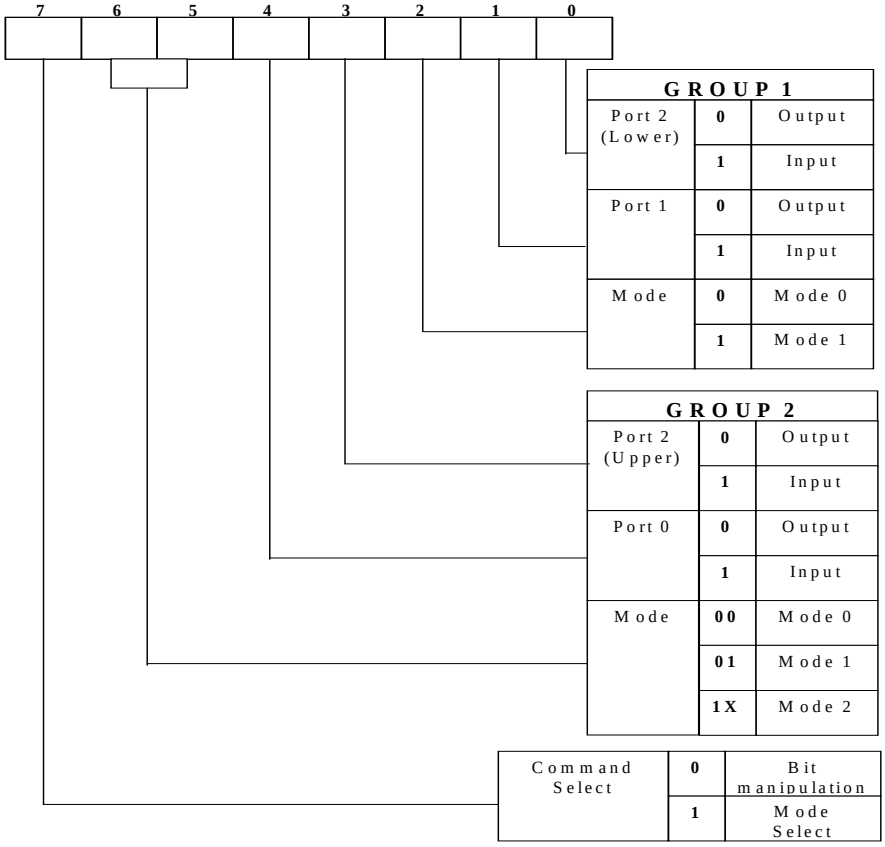


Figure 3.1 Mode Select Command Word

P50 maps U1, the PPI 8255, at base I/O address PPI = 0x1800.

All ports/registers are offsets of this I/O base address.

The Command Register address = PPI1+3; Port 0 address = PPI+0; Port 1 address = PPI1+1;

and Port 2 address = PPI1+2.

The following code example will set all ports to output mode:

```
outportb(PPI+3,0x80);  /* Mode 0 all output selection. */
```

And then write to specific pins after setup:

```
outportb(PPI+0,0x55);  /* Sets port 0 to alternating high/low I/O pins. */
outportb(PPI+1,0x55);  /* Sets port 1 to alternating high/low I/O pins. */
outportb(PPI+2,0x55);  /* Sets port 2 to alternating high/low I/O pins. */
```

To set all ports to input mode:

```
outportb(PPI1+3,0x9f);     /* Mode 0 all input selection. */
```

You can read the ports with:

```
inportb(PPI1+0); /* Port 0 */
inportb(PPI1+1); /* Port 1 */
inportb(PPI1+2); /* Port 2 */
```

These *inport(PPI+i);* statements return an 8-bit value for each port, with each bit corresponding to the appropriate line on the port.

There are 24 TTL level I/O pins free to use for your application. These I/O lines are specified as 4 mA driving current capability. See schematics for PPI connection header J3 .

3.3.3 HCTL2020

Two quadrature decoder/counter interface chips, (HCTL2020, Hewlett Packard, U6 and U8) can be installed on the P50. The quadrature decoder is used to interface incremental motion encoders with the microprocessor system or to improve system performance for digital closed-loop motion control systems. The HCTL2020 includes a quadrature decoder, a 16-bit counter, and an 8-bit bus interface. It features full 4x decoding, up to 14 MHz clock operation, high noise immunity due to Schmitt-trigger inputs and digital noise filters, quadrature decoder output signals, up/down signal, count signals, and cascade output signal. Many types of optical incremental encoder modules, such as the HEDS-9000, HEDS-9100, and HEDS-9200 from HP, can be directly interfaced to the HCTL2020.

Channel A and B signals buffered with Schmitt trigger inputs (U7, 74HC14, CHA1/2, CHB1/2) are routed at pin 30, 32, 35, and 36 on headers H5. The HCTL2020 has built-in filters, which allow reliable operation in noisy environments.

3.3.4 AD7852,Parallel 12-bit ADC

The AD7852 is a 100 ksps, sampling parallel 12-bit A/D converter that draws only 55 mW from a single 5V supply. This device includes 8 channels with sample-and-hold, precision 2.5V internal reference and switched capacitor successive-approximation A/D.

The input range of the AD7852 is 0-5V. Four channels are routed to ops (LM324S, U16) to provide differential input. Maximum DC specs include ±2.0 LSB INL and 12-bit no missing codes over temperature. The ADC has a 12-bit data parallel output port that directly interfaces to the full 12-bit data bus D11-D0 for maximum data transfer rate.

The AD7852 does require an external clock. It requires 16 ADC clocks to complete one conversion. The 586-Engine provides the necessary clock for the ADC via CLKT (J1.4). By default the CLKT is programmed to provide a 1.8432 MHz ADC clock. The busy signal has a low period indicating that conversion is in progress, however, no connections are made to this pin. In order to achieve maximum sample rate, the 586-Engine must use polling method, not interrupt operation, to acquire parallel ADC data with an inport(); instruction. A sample program **p50_ad.c** can be found in the **`c:\tern\586\samples\p50`** directory.

3.3.5 DA7625, Parallel 12-bit DAC

The DA7625 is a parallel 12-bit D/A converter. This device supports 4 voltage output channels buffered by ops with hardware configurable gain (default gain=2), giving defualt output range of 0-5V. An on-board pot allows for adjustable analog output voltage. It accepts 12-bit parallel input data and has double-buffered DAC input logic.It requires an external 2.5V reference which is provided on the 586-Engine.

The 586-Engine uses data bus D11 to D0 to directly interface to the DAC's full 12-bit data bus for maximum data transfer rate. The DA7625 has a settling time of 5 µs. A sample program **p50_da.c** is in the **`c:\tern\586\samples\p50`** directory.

3.3.6 Ethernet

The Ethernet LAN Controller on the P50 is the CS8900 from Crystal Semiconductor Corporation (512-445-7222). The CS8900 includes on-chip RAM and 10BASE-T transmit and receive filters. The CS8900 directly interfaces to the TERN controller's data bus, providing a high-speed, full duplex operation. The P50 interface to the Ethernet is via a standard RJ45 8-pin connector (J6). The CS8900 offers a broad range of performance features and configuration options. Its unique PacketPage architecture automatically adapts to changing network traffic patterns and available system resources. The CS8900-based P50 can increase system efficiency and minimize CPU overhead in a 10BASE-T network. The P50 with CS8900 provides a true full-duplex Ethernet solution, incorporating all of the analog and digital circuitry needed for a complete C/C++ programmable Ethernet node controller.

3.3.7 Opto-couplers

There are 8 opto-couplers at the J4 header. These opto-couplers provide optical isolation and can be used for digital inputs, relay contact monitor, or powerline monitor. These optos have a 3 micro-second ON time and 5 micro-second OFF time. The on-board input pins have a 1kΩ pullup, so a low input signal will turn the coupler ON.

3.3.8 High-Voltage, High-Current Drivers

ULN2003 (U13 and U14) are high voltage, high current Darlington transistor arrays, consisting of 7 silicon NPN Darlington pairs on a common monolithic substrate. All channels feature open-collector outputs for sinking 350 mA at 50V, and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA sinking are allowed. Outputs may be paralleled to achieve high-load capability, although each driver has a maximum continuous collector current rating of 350 mA at 50V. The maximum power dissipation allowed is 2.20 W per chip at 25 degrees C. The common substrate G is routed to J4 GND pins. All currents sinking in must return to the J8 GND pins (J8 pin 9, 19,20). A heavy gage(20) wire must be used to connect the J8 GND terminal to an external common ground return. K connects to the protection diodes in the ULN2003 chips and should be tied to highest voltage in the external load system. K can be connected to an unregulated on board +12V. **ULN2003 is a sinking driver not sourcing driver.** Typical application wiring is shown below.

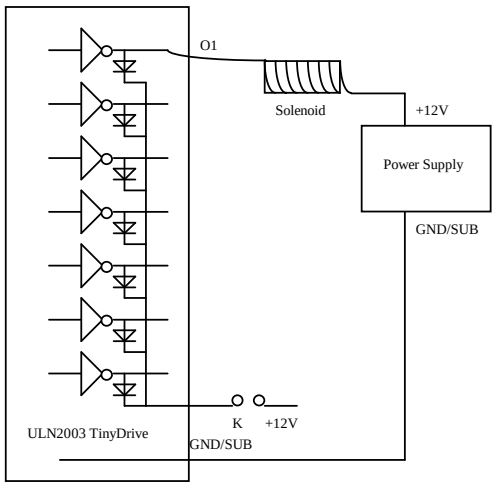


Figure 3.2 Drive inductive load with high voltage/current drivers.

3.4 Headers and Connectors

3.4.1 Expansion Headers J1 and J2

Two 20x2, 0.1 spacing sockets are installed on the P50 for 586-Engine installation. Most signals are directly routed to the 586-Engine processor. *These signals are 3.3V output and 5V input tolerant ONLY, and any out-of-range voltages will most likely damage the board.*

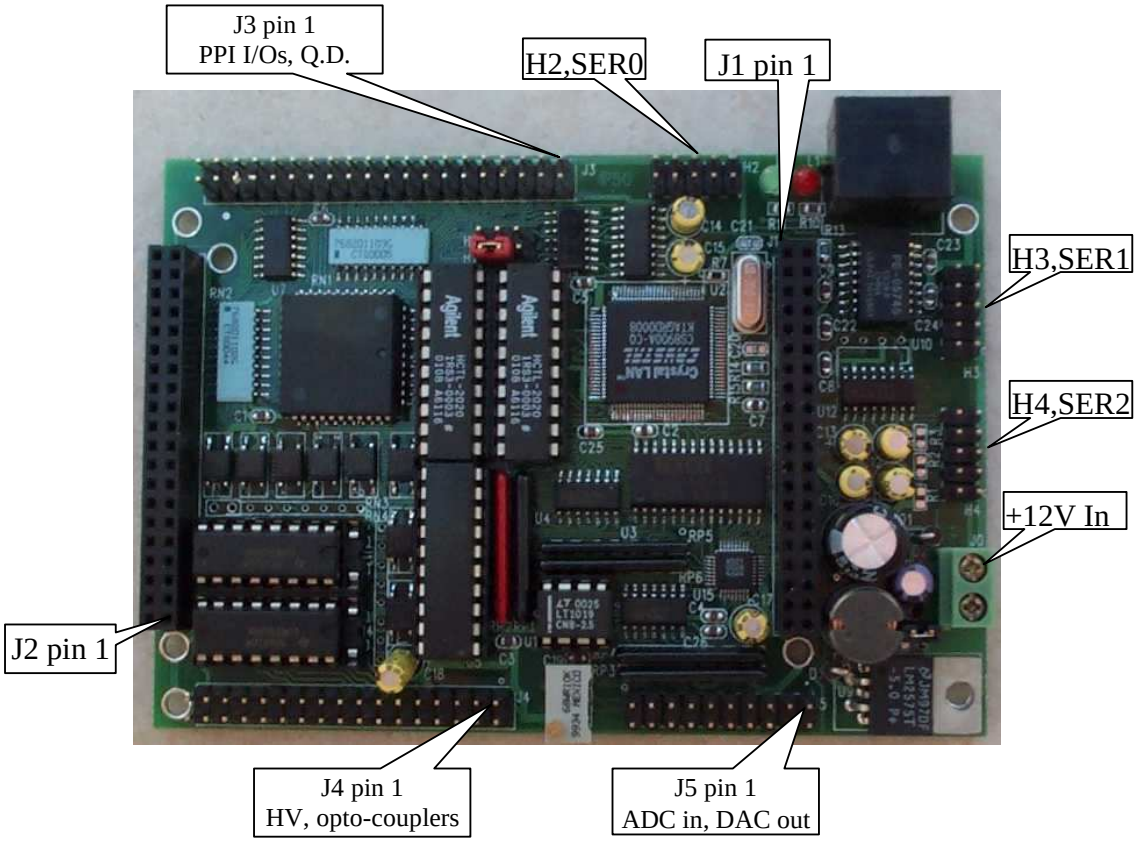


Figure 3.3 Pin header locations and descriptions

J1 Signal				*J2 Signal*			
VCC	1	2	GND	GND	40	39	VCC
MPO	3	4	CLK	P31	38	37	P27
RxD	5	6	GND	P28	36	35	P29
TxD	7	8	D0	TxD0	34	33	P23
VOFF	9	10	D1	RxD0	32	31	/RTS1
	11	12	D2	P30	30	29	P26
	13	14	D3	TxD1	28	27	/RTS0
/RST	15	16	D4	RxD1	26	25	P25
RST	17	18	D5	P24	24	23	P22
/CS6	19	20	D6	/CTS1	22	21	P21
	21	22	D7	P19	20	19	P20
	23	24	GND	P17	18	17	P18
	25	26	A7	P15	16	15	P16
	27	28	A6	P11	14	13	P12
/WR	29	30	A5	P9	12	11	P10
/RD	31	32	A4	P7	10	9	P8
D11	33	34	A3	P13	8	7	P6
D10	35	36	A2	P14	6	5	P5
D9	37	38	A1	P2	4	3	P4
D8	39	40	A0	GND	2	1	P3

Table 3.1 J1 and J2, 20x2 expansion ports for P50

Signal definitions for J1:

VCC	+5V power supply
GND	Ground
CLK	Software programmable clock output from AMD SC520, used by ADC on P50, see 586_ad.c for example on selecting clock speed
RxD	data receive of UART SCC2691, U8 on 586-Engine
TxD	data transmit of UART SCC2691, U8 on 586-Engine
MPO	Multi-Purpose Output of SCC2691, U8 on 586-Engine
VOFF	real-time clock output
D0-D11	AMD SC520 external data bus
A7-A0	AMD SC520 lower address lines
/RST	reset signal, active low
RST	reset signal, active high
/CS6	8-bit chip select on the 586-Engine, not used by P50
/WR	active low when write operation
/RD	active low when read operation

Signal definitions for J2:

VCC	+5V power supply
GND	Ground
Pxx	AMD SC520 PIO pins
TxD0	AMD SC520 transmit data of serial channel 0
RxD0	AMD SC520 receive data of serial channel 0
TxD1	AMD SC520 transmit data of serial channel 1

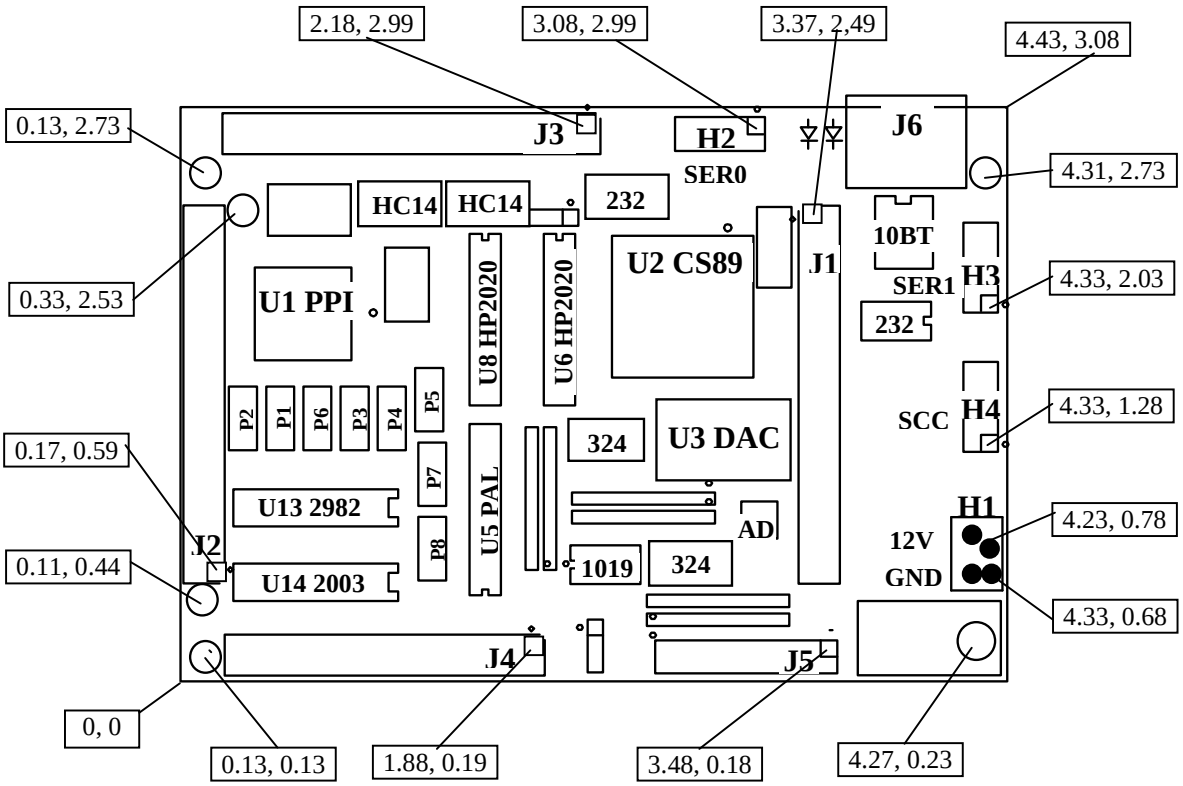
RxD1	AMD SC520 receive data of serial channel 1
/CTS1	AMD SC520 Clear-to-Send signal for SER1
/RTS0	AMD SC520 Request-to-Send signal for SER0
/RTS1	AMD SC520 Request-to-Send signal for SER1
P31	J2 pin 38 Used as Step Two jumper

3.4.2 Jumpers and Headers

The jumpers and connectors on the P50 are listed below.

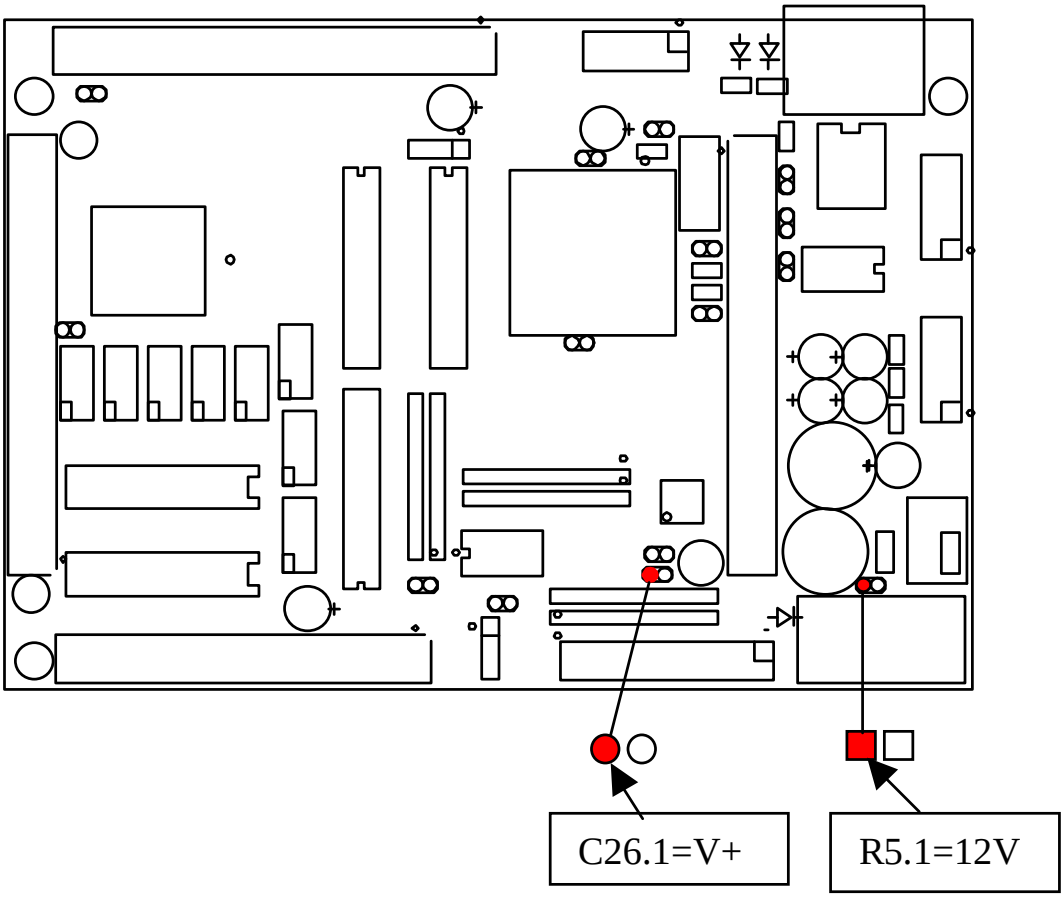
Name	**Size**	**Function**	**Possible Configuration**
J1	20x2	main expansion port	(same as the 586-Engine)
J2	20x2	main expansion port	(same as the 586-Engine)
J3	20x2	PPI TTL I/Os / Q.D. signals	PPI(U1), Q.D.(U6 and U8)
J4	17x2	HV and opto-couplers	HV(U13 and U14), opto (P1-P8)
J5	10x2	ADC and DAC lines	ADC(U15) , DAC(U3)
J6	4x2	Ethernet interface connection	U2
H1	2x1	+12V power input	
H2	5x2	SER0 (DEBUG), RS232	
H3	5x2	SER1, RS232	
H4	5x2	SCC2691: RS232/485 TXD, RXD, GND	Install RS232 or RS485 driver for 3rd UART on the 586-Engine
H5	3x1	reference voltage selector	
H6	3x1	Interrupt selector for Ethernet interface	based on which controller is used to drive P50
H7	3x1	chip select selector	586-Engine, jumper on pins 1&2 AE-86 or i386-Engine, jumper on pins 2&3

Appendix A: P50 mechanical dimensions

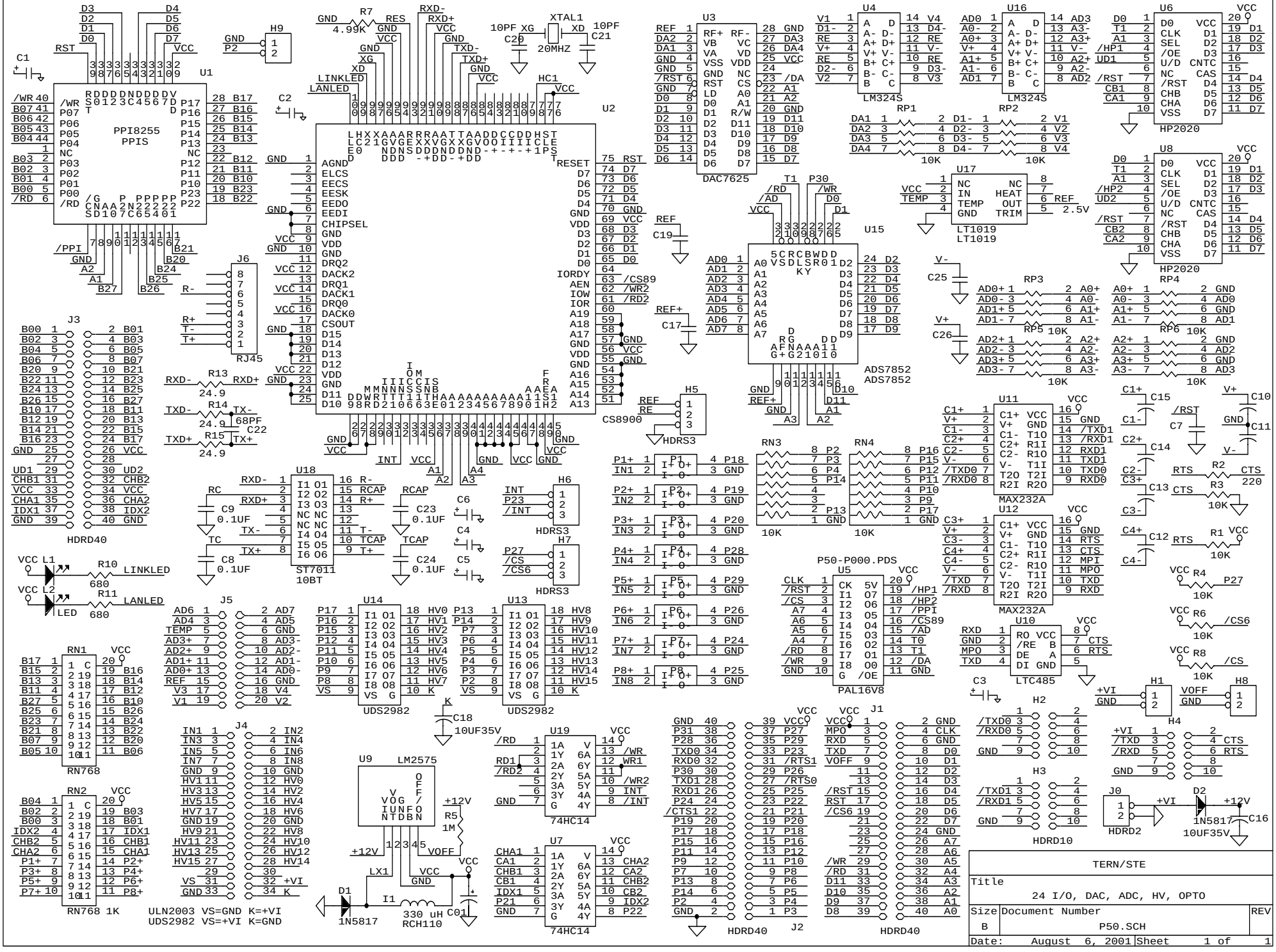


Appendix B: Modification on P50

for 0-10 V DAC outputs and 0-10V ADC inputs.



1) Add wire from C26.1=V+ to R5.1=12V.
   Note: Power to the P50 should be with in 12V-15V.
2) For DAC 0-10V outputs
   GAIN=4, RP1=5K, RP2=20K
3) For ADC 0-10V inputs
   GAIN=1/2, RP4=RP6=10K, RP3=RP5=20K


U1
PPI8255
PPIS
U2
LM2575
U3
DAC7625
U4
LM324S
U16
LM324S
U6
HP2020
U8
HP2020
U15
ADS7852
ADS7852
U17
LT1019
LT1019
U18
ST7011
10BT
U11
MAX232A
U12
MAX232A
U14
UDS2982
U13
UDS2982
U5
PAL16V8
U10
LTC485
U19
74HC14
U7
74HC14
J1
J2
J3
J4
J5
J6
J0
H1
H2
H3
H4
H5
H6
H7
H8
H9
RN1
RN768
RN2
RN768 1K
RN3
RN4
RP1
RP2
RP3
RP4
RP5 10K
RP6 10K
HDRD40
HDRD10
HDRD2
HDRS3
RJ45
CS8900
LED
D1
1N5817
1N5817
ULN2003 VS=GND K=+VI
UDS2982 VS=+VI K=GND
330 uH
RCH110
P50-P000.PDS
TERN/STE
24 I/O, DAC, ADC, HV, OPTO
P50.SCH
August 6, 2001