PC-Co™

PC ISA Controller with upto **100** I/O, **4** serial ports, and **3** power relays

Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1
Introduction

1.1 Functional Description

The PC-Co™ is a low-cost C/C++ programmable industrial embedded controller with up to 100 I/O lines and a PC-ISA bus. You may use the PC-Co™ as a standalone controller or install it in a PC ISA slot as a co-processor board. It contains three power relays (5 A). It also has four solenoid drivers, each capable of sinking up to 350 mA inductive load at 50V. Three 82C55 PPIs provide 72 lines of bi-directional TTL level I/O. An interface supports many types of character or graphic LCD modules. The PC-Co™ can be configured with up to four channels of serial ports, including two V25 internal UARTs, one external SCC2691 on the C-Engine™ and one SCC2691 on the PC-Co™.

You may have four channels of RS-232 ports routed to the DB9 connector. Two ports can be replaced with RS-485 drivers. A DB25 connector provides three power relay contacts (NC, NO, COM), four solenoid drivers, and nine TTL I/O lines from V25. A total of 72 bi-directional I/O lines from 3 PPI chips are routed to two 40-pin headers. The ISA edge connector can provide eight I/O lines in the standalone mode.

The PC-Co™ must be driven by a V25-Engine™, or C-Engine™, or A-Engine™ .

The host C-Engine™ also provides 11 channels of 12-bit ADC, 24 I/O lines, 2 RS232 serial ports, and one UART(SCC2691) for multi-drop RS485 networking. An optional 4th serial port (SCC2691) can be installed on the PC-Co. The two SCC2691 UART can be configured as either RS232 or RS485 ports.

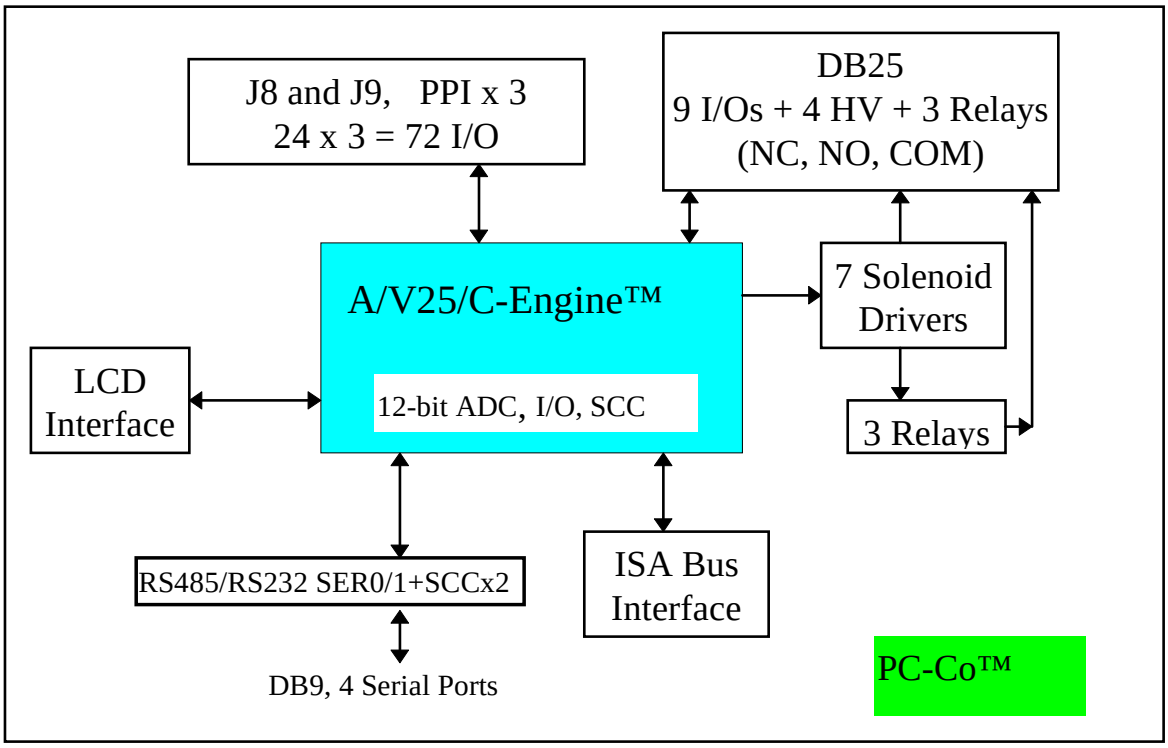


Fig. 1.1, Functional block diagram of the PC-Co™ and the C-Engine™.

1.2 Minimum Requirements

The minimum hardware requirements are:
* PC-Co™, including a V25-Engine™ or C-Engine™.
* A serial cable (PC-V25) with a DB9 Conector and an IDC10 Conector.
* Center negative wall transformer (+9 V, 500 mA); and a PC or PC compatible computer.

The minimum software requirements are:
* Microsoft Visual C/C++ and MASM611,
  or Borland C/C++(3.1, 4.0, 4.5) , Turbo C/C++ 3.0 and TASM;
* TERN C/C++ Evaluation Kit(EV-C) or C/C++ Development Kit (DV).

FEATURES

- 4.9x4.2 inches
- Power consumption: <200 mA, on-board +5V regulator
- Borland or Microsoft C/C++ programmable
- Up to 100 I/O lines including 24x3 PPI I/O lines
- Up to 4 RS232 serial channels, RS485 for networking
- 4 channels of high-voltage outputs
- 3 power relays with normal open, normal close, COM
- Character or graphic LCD interface
- PC 8-bit ISA bus edge connector
- Driven by a C-Engine™ or a V25-Engine™
- EPROM (32K, up to 512K) and SRAM (32K, up to 512K)
- Battery backup for memory and real-time clock
- Watchdog and power-fail protection
- 11 channels of 12-bit ADC with C-Engine™

How to program the PC-Co™ ?

You program the PC-Co™ from your PC via serial link. You can use your favorite Borland or Microsoft C/C++ compilers. Your C/C++ program can be remotely debugged on the PC-Co™ over serial link at 115,000 baud rate. TERN provides I/O driver libraries, sample programs, target EPROMs, batch files, and all the hardware necessary for you to quickly develop your application software. For more details please see the data sheet and Technical Manual for the C-Engine™.

Chapter 2
Installation

2.1 Software Installation

See V25-Engine™ or C-Engine™ manual for software installation.

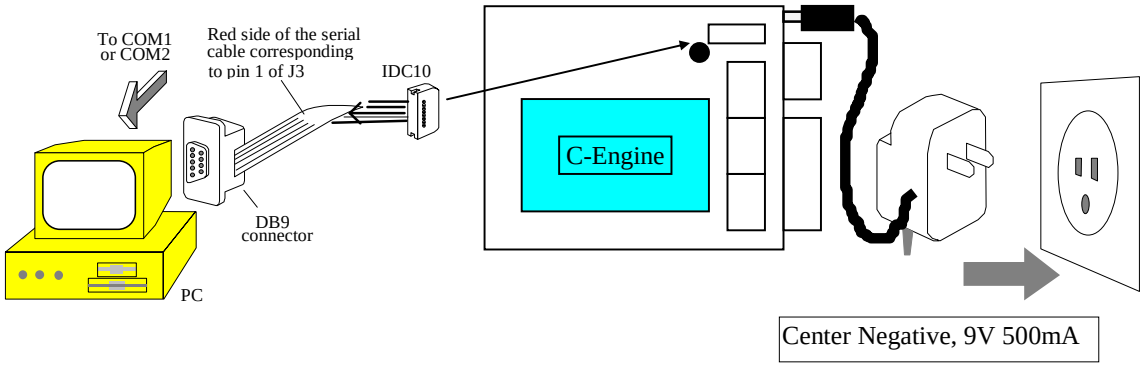


Fig. 2.1. Connect the PC-Con™ to your PC COM1/2 via a PC-V25 serial cable.

2.2 Hardware Installation

1. Connect the IDC10 connector of the RS232 serial cable to J6 of PC-Co™, with the red side of the cable corresponding to pin 1 of J6 (a small circle close to J6 indicates pin number 1), and connect DB9 connector of the serial cable to COM1 or COM2, the PC serial port, as shown in Fig. 2.1.
Connect a center negative wall transformer (+9V DC) to the PC-Co™ DC power jack J4.

2.3 Simple Test

At power on, while the LED blink twice, the power relay driven by the P05 line will click twice. You can run a simple sample program "**led.c**" under your default directory to test the software and hardware installation. The LED on the C-Engine™ should blink if everything is installed correctly. The procedure involved in the test is described in the V25-Engine™/C-Engine™ Manual.

2.4 Sample Programs

You may test sample programs under samples\pc directory.
pc_ppi.c pc_hv.c alarm.c pc_scc.c
pc_relay.c

Chapter 3
Hardware

3.1 V25-Engine™, C-Engine™, or A-Engine™

The PC-Co™ uses a V25-Engine™, or a C-Engine™ or an A-Engine™ as its microprocessor core module. Please refer to the V25-Engine™, C-Engine™, or A-Engine™ Technical Manual for more information.

3.2 Interface with the C-Engine™, V25-Engine™, or A-Engine™

The C-Engine™ or V25-Engine™ must be installed with the 84 pin PLCC V25 CPU next to the power relays. The A-Engine™ must be installed with the Am188ES CPU and the battery next to the power relays.

3.3 PC-Co I/O Map

The following tables list the I/O address of the PC-Co™, together with their Data Bits, Chip-Select Symbol and Functions.

Address	Data Bits	Select Symbol	Function
0x10	D0-7	/PPI1	U8, PPI1 chip enable for D0-7 to access PPI registers.
0x20	D0-7	/PPI2	U7, PPI2 chip enable for D0-7 to access PPI registers.
0x30	D0-7	/PPI3	U6, PPI3 chip enable for D0-7 to access PPI registers.
0x40	D0-D7	/VRD	V25 Reads the ISA buffer input register, U4
0x50	D0-D7	/VWR	V25 Writes D0-7 to the ISA output buffer register, U5
0x80-0x9f	D0-7	LCD1	Write/Read D0-7 to LCD1, at J14 pin 9 and J13 pin 7.
0xa0-0xb7	D0-7	LCD2	Write/Read D0-7 to LCD2, at J14 pin 15 and J13 pin 10.
0xc0-0xdf	D0-7	/SCC2	U9 of the PC-Co™, UART SCC2691 chip enable.

3.4 High-voltage, High-current Drivers

U14, ULN2003 has high voltage, high current Darlington transistor arrays, consisting of 7 silicon NPN Darlington pairs on a common monolithic substrate. All channels feature open-collector outputs for sinking 350 mA at 50V, and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA sinking are allowed. The outputs may be paralleled to achieve high-load capability, although each driver has a maximum continuous collector current rating of 350 mA at 50V.
The maximum power dissipation allowed is 2.20 W per chip at 25 degree C. The common substrate G is routed to J3 DB25 pin11 GND. All currents sinking in must be return from J3 pin 11 GND. A heavy gage(20) wire may be used to connect GND terminal to external power supply ground return. K is connecting to the protection diodes. K should be tied to highest voltage in the external load system. K is connected to J3 pin 24.

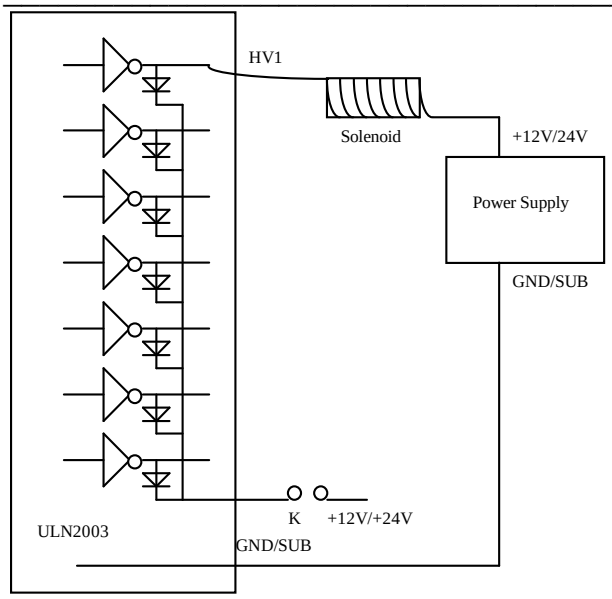


Fig. 3.3 Drive inductive load with high voltage/current drives.

ULN2003 is a sink driver not sourcing driver. A typical application wiring is shown in Fig. 3.3
Three power relays are driven by the ULN2003.

The ULN2003 is driven by V25 I/O pins via J2 connector.
The P05 line is shared by the LED.
The P14, P16 have been used as RS-232 handshaking lines (RTS), in some of V25-Engine applications.

You can control the ULN2003 solenoid drivers with ***pc_hv(char relay, char on_off);***
where relay=1-7 for solenoid drivers HV1-7 of the U14;
hv=1-3 are driving relay 1-3
dat=0/1, off/on

3.5 SCC2691 UART, RS-232 and RS-485 drivers

The U9 SCC2691 UART(SCC2) is on the PC-Co™, in additional to the SER0, SER1 from V25 CPU, and a SCC2691 UART (SCC) on the VE/CE. There are a total of 4 serial ports.
SER0 and SER1 are always configured as RS-232 without handshaking. SCC and SCC2 can be configured as RS-232 or RS-485. The defaults are RS-232. If you install a RS-485 driver (75176) for SCC in U11, you must cut the pin 11 of U13 off, in order to disable RS-232 receiving signal into RxD of SCC. If you install a RS-485 driver (75176) for SCC2 in U16, you must cut the pin 8 of U13 off, in order to disable RS-232 receiving signal into RxD2 of SCC2.

3.6 ISA Interface

There is a 31 pin board edge connector. You may install the PC-Co into a 8-bit ISA bus slot in a PC. The PC-Co only uses the +12VI from PC and generates +5V on its own regulator. There are 2 buffer register (74HC374, U4, and U5). The V25, as a co-processor for the PC, reads the 8-bit buffer from U4, and writes the 8-bit buffer of U5. The PC can always reads the U5 and writes to U4.
PAL(PC0210) in U2 and PAL(PCP020) in U1 are designed for decoding PC I/O mapped access and additional commands which can be read by V25 PT0-3. It also can generates an interrupt to the V25 via P13.
The PAL equation are listed below.

```
Title PCP010_PC DESIGN
Pattern PCP010.pds
Revision A
Company  TERN, DAVIS, CA
Date     1/14/96
; PC CONTROLLER.U2
CHIP  PAL_AMD   PALCE16V8

;PINS  1    2    3    4    5    6    7    8    9    10
    /IOW   SD3   SD2   SD1   SD0   /PA   SA1   SA0   /IOR   GND
;PINS  11    12    13    14    15    16    17    18    19    20
     /OE   /PWR  /P13   PT0   PT1   PT2   PT3   /RST  /PRD  VCC

EQUATIONS

PWR = IOW*/IOR* PA*/SA1* SA0                    ; XX XXXX XX01
PRD = IOR*/IOW* PA*/SA1* SA0                    ; XX XXXX XX01
P13 = IOW*/IOR* PA* SA1*/SA0            ; XX XXXX XX10
P13.TRST = /P13                         ;OUTPUT LOW ONLY

RST = IOW*/IOR* PA*/SA1*/SA0            ; XX XXXX XX00
RST.TRST = /RST                         ;OUTPUT LOW ONLY

PT0 = IOW*/IOR* PA* SA1* SA0* SD0
          + PT0*/IOW
          + PT0* IOR
          + PT0*/PA
          + PT0*/SA1
          + PT0*/SA0                    ; XX XXXX XX03
PT1 = IOW*/IOR* PA* SA1* SA0* SD1
          + PT1*/IOW
          + PT1* IOR
          + PT1*/PA
          + PT1*/SA1
          + PT1*/SA0                    ; XX XXXX XX03
PT2 = IOW*/IOR* PA* SA1* SA0* SD2
          + PT2*/IOW
          + PT2* IOR
          + PT2*/PA
          + PT2*/SA1
          + PT2*/SA0                    ; XX XXXX XX03
PT3 = IOW*/IOR* PA* SA1* SA0* SD3
          + PT3*/IOW
          + PT3* IOR
          + PT3*/PA
          + PT3*/SA1
          + PT3*/SA0                    ; XX XXXX XX03
```

Title PCP020_PC DESIGN

```
Pattern PCP020.pds
Revision A
Company  TERN, DAVIS, CA
Date     1/12/96
; PC CONTROLLER.U1=74HC688
;I/O 0x200 0x210 0x2f0 0x300 0x310 0x380 0x3e0
CHIP  PAL_AMD   PALCE16V8

;PINS 1    2    3    4    5    6    7    8    9    10
    /NN   PC9   SA9   PC8   SA8   PC7   SA7   PC6   SA6    GND
;PINS 11   12   13   14   15   16   17   18   19   20
    PC2   SA2   PC4   SA4   PC3   SA3   PC5   SA5   /PA   VCC

EQUATIONS
PA=PC9*SA9*/PC8*/SA8*/PC7*/SA7*/PC6*/SA6*/PC5*/SA5*/PC4*/SA4*/PC3*/SA3
+PC9*SA9*/PC8*/SA8*/PC7*/SA7*/PC6*/SA6*/PC5*/SA5*PC4*SA4*/PC3*/SA3
+PC9*SA9*/PC8*/SA8*PC7*SA7*PC6*SA6*PC5*SA5*PC4*SA4*/PC3*/SA3
+PC9*SA9*PC8*SA8*/PC7*/SA7*/PC6*/SA6*/PC5*/SA5*/PC4*/SA4*/PC3*/SA3
+PC9*SA9*PC8*SA8*/PC7*/SA7*/PC6*/SA6*/PC5*/SA5*PC4*SA4*/PC3*/SA3
+PC9*SA9*PC8*SA8*PC7*SA7*/PC6*/SA6*/PC5*/SA5*/PC4*/SA4*/PC3*/SA3
+PC9*SA9*PC8*SA8*PC7*SA7*PC6*SA6*PC5*SA5*/PC4*/SA4*/PC3*/SA3
```

3.7 LCD Interface

You can interface a character type LCD or graphic LCD to the PC-Co. There are two headers, J13, and J14, on the PC-Co providing D0-D7, A0, LCD1, and other LCD interface signals. You may use V25-Engine™, or C-Engine™ to interface to LCDs via J13 or J14, Not the A-Engine™. The 40 MHz high speed data bus of the A-Engine™ is too fast to directly interface to most LCD modules. You may use PPI I/O lines to interface with LCDs.

The default PAL in U3 is a PCP000.

The PCP000 PAL in U3 will provide active high LCD1 and LCD2 signal, typical for character LCDs.

The PCP100 PAL in U3 will provide active low LCD1 and LCD2 signal, typical for graphic LCDs.

Chapter 4
Software

4.1 Programming in Microsoft/Borland C/C++

Please refer to the C-Engine™ Technical Manual for more details.

4.2 Sample program and Functions

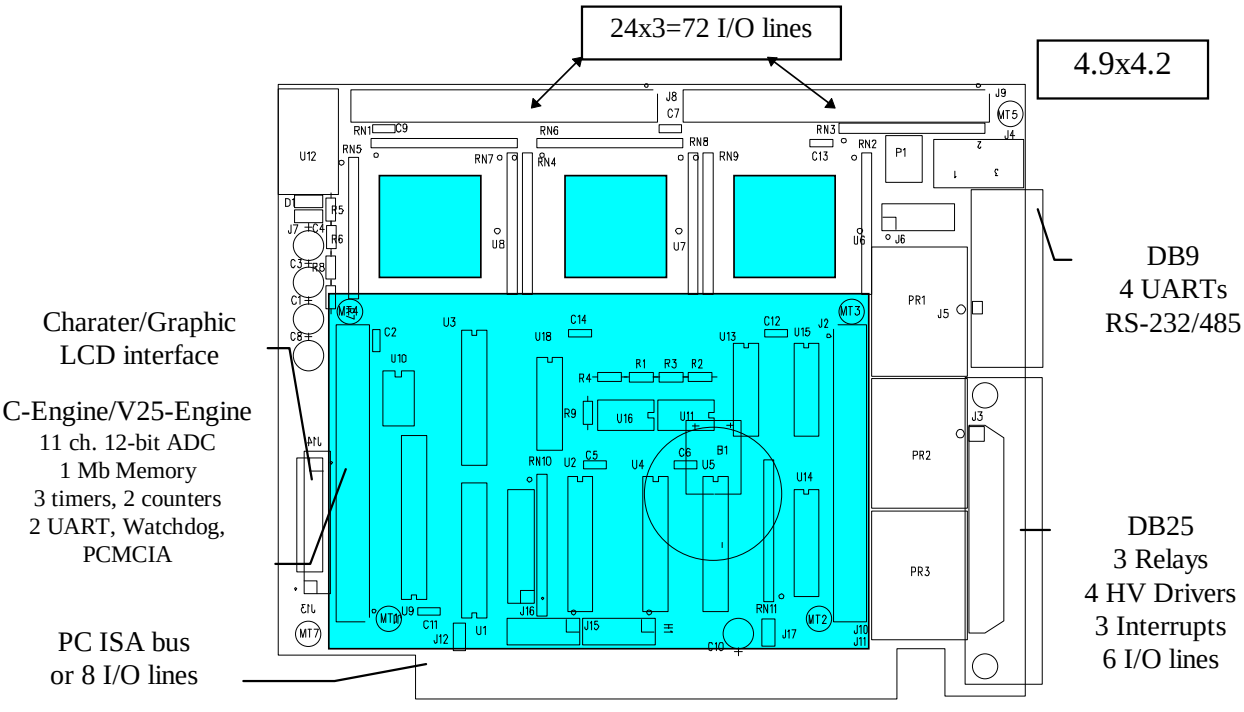
void ***pc_hv***(char hv, char onoff); // Solenoid drivers

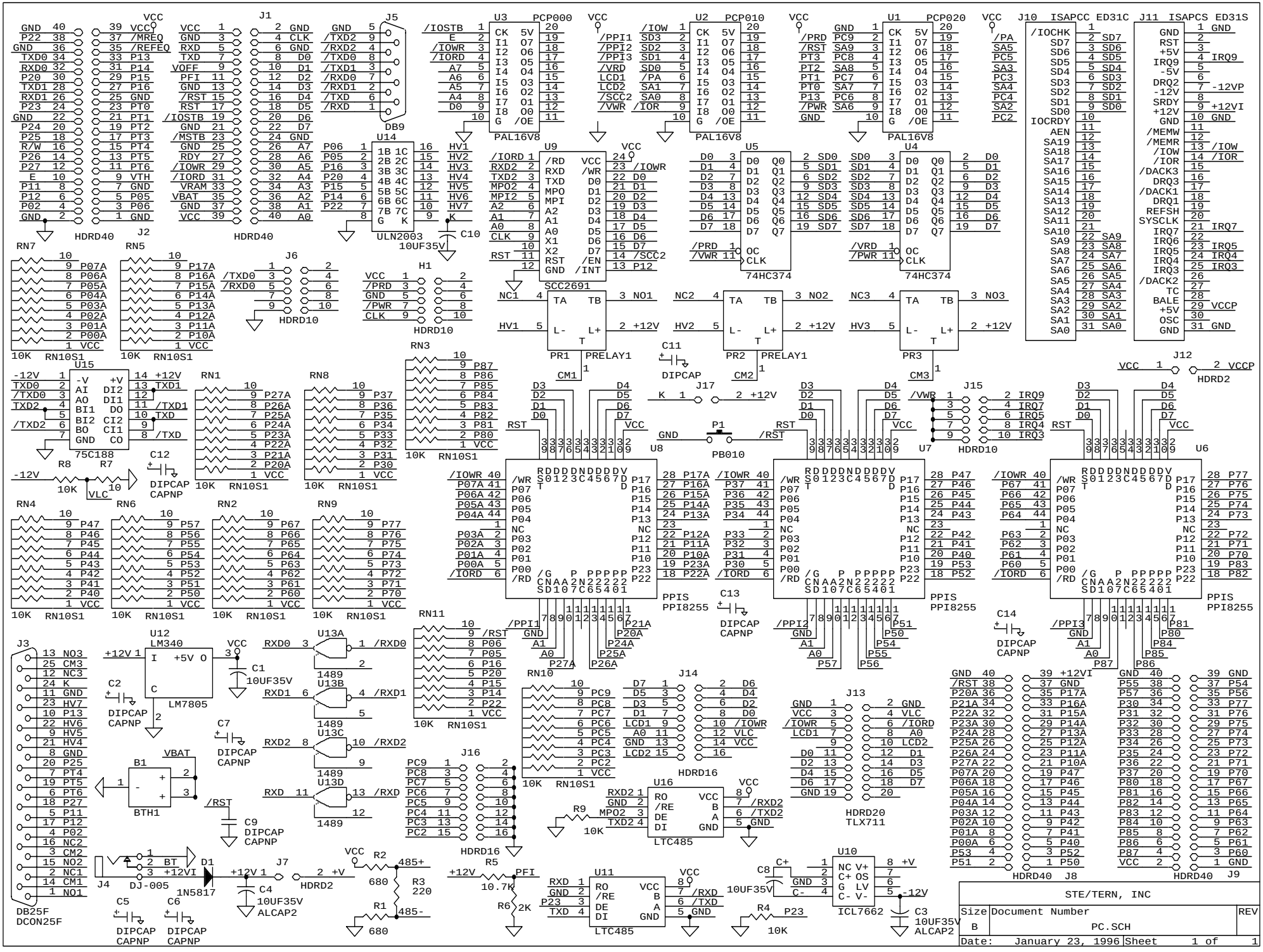
void ***pc_relay***(char relay, char onoff); // power relays

UART SCC2 is the same as the UART SCC2 in the BirdBox. Please see scc2.h abd samples/bb/bb_scc2.c

See pc_ppi.c and alarm.c

Appendix A: PC-Co™ Layout




J1
J2
J5
DB9
U3 PCP000
U2 PCP010
U1 PCP020
PAL16V8
J10 ISAPCC ED31C
J11 ISAPCS ED31S
HDRD40
U14
ULN2003
C10
10UF35V
U9
SCC2691
U5
U4
74HC374
J6
HDRD10
H1
U15
75C188
R8
R7
C12
DIPCAP
CAPNP
U8
PB010
U7
HDRD10
U6
PPIS
PPI8255
J12
HDRD2
C11
C13
C14
RN1
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
RN10
RN11
10K RN10S1
10K RN10S2
J3
DB25F
DCON25F
U12
LM340
LM7805
C1
C2
U13A
U13B
U13C
U13D
1489
B1
BTH1
C7
C9
J16
HDRD16
U16
LTC485
R9
J14
J13
HDRD20
TLX711
J4
DJ-005
D1
1N5817
J7
C4
C5
C6
R2
R1
R3
R5
R6
U11
U10
ICL7662
C8
R4
C3
J8
J9
STE/TERN, INC
Size B
Document Number PC.SCH
REV
Date: January 23, 1996
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