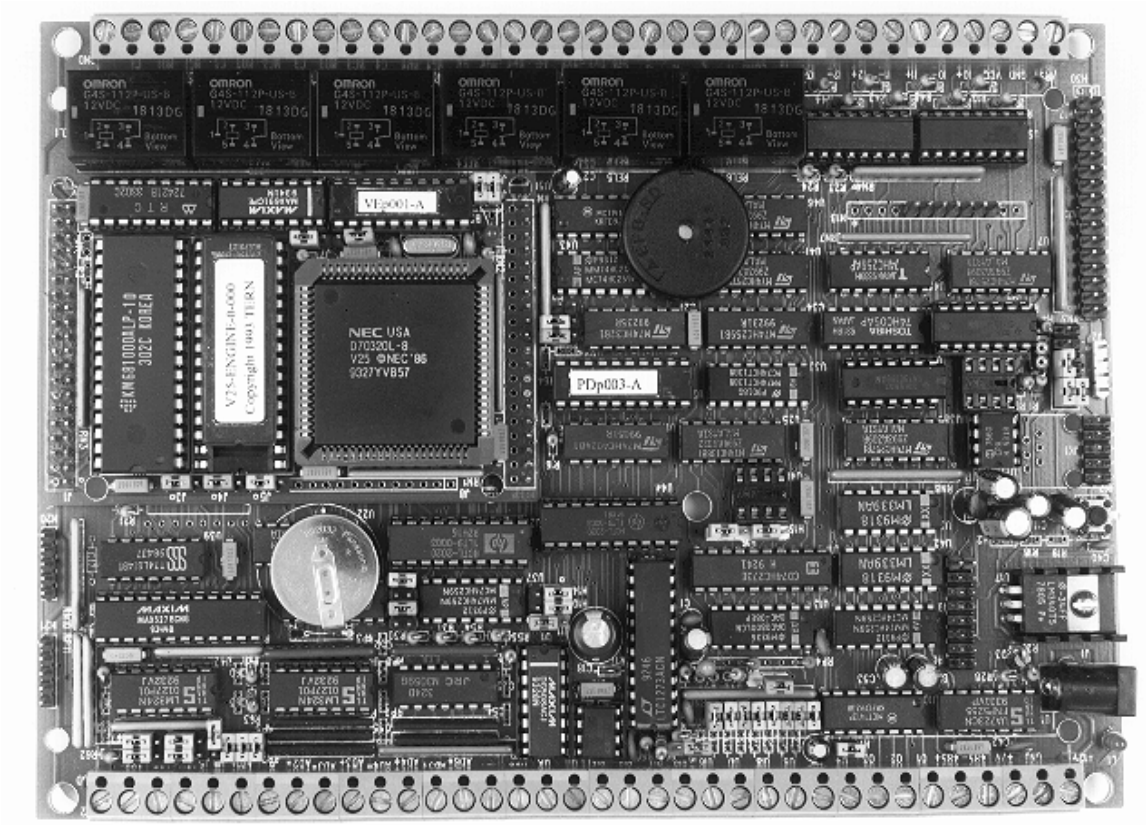
PowerDrive™

A Complete Solution
for
Many Data Acquisition and Control Applications



Technical Manual

TERN INC.
1950 5th Street, Davis, CA 95616, USA
Tel: 530-758-0180 Fax: 530-758-0181
Email: sales@tern.com http://www.tern.com

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TERN INC.
1950 5th Street, Davis, CA 95616, USA
Tel: 530-758-0180 Fax: 530-758-0181
Email: ***sales@tern.com*** ***http://www.tern.com***

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1
Introduction

1.1 Functional Description

The PowerDrive™ from TERN is a compact, reliable, high performance, low cost, complete solution for many data acquisition and control applications. Driven by a V25-Engine™ or a C-Engine™, the PowerDrive™ features numerous peripherals on a single PCB measuring 7.9x5.6 inches. In additional to the features of the V25-Engine™ or C-Engine™, the PowerDrive™ features 8 channels of high-speed 12-bit ADC (LTC1272, 3/5/8µs, on-chip sample-and-hold and reference), 4 channels of fast-settling 12-bit DAC (MAX527, 5µs settling, 1 LSB error), 7 channel high voltage/current driver that can sink 300 mA each channel, 16 digital inputs, 10 digital outputs, 8 comparator inputs which take either analog (10-bit resolution) or digital inputs, 6 power relays with normal-open, normal-close, and common pins connecting to terminal blocks that can handle at least 5A current, 8 opto-couplers which take either AC or DC high voltage inputs, two RS-232 serial ports, one RS-485 serial port for networking, and two HP quadrature decoders (HP2020), which can directly interface to external optical encoders for motion control. The decoders (HP2020) also can be used as high-speed 16-bit counters up to 10MHz. Schmitt-trigger inverters are provided for high-speed counter inputs, to increase noise immunity and transform slowly-changing input signals to fast-changing, jitter-free output signals. The on-board power supply converts a single input 12V voltage to +5V, -12V, -5V, +7V, and reference voltage, to operate the on-board hardware. An analog signal-conditioning circuit provides the user with 8 channels of configurable gain, filter and buffer Ops. The output signal from the signal-conditioning circuit may be used to construct eight channels of 10-bit ADC without using the 12-bit ADC. A LCD interface, a 5x8 keypad interface, and a PDC (Portable Data Carrier) port is on-board. The 72-position terminal block allows easy access to PowerDrive™ signals.
You can use your favorite Borland or Microsoft C/C++ compilers to program the PowerDrive™ from a PC. Your program can be remotely debugged on the PowerDrive™ using Paradigm DEBUG over a serial link at 115,000 baud rate. TERN provides I/O libraries, sample programs, target EPROM, batch files, and all the hardware necessary for users to quickly develop their application software. For more details please see the data sheet and Technical Manual for V25-Engine™ or C-Engine™.

1.2 Minimum Requirements

The minimum hardware requirements are:
□PowerDrive, including a V25-Engine™ or C-Engine™ with DEBUG EPROM (C-Core-0-xxx-E).□
A serial cable (PC-V25) with a DB9 connector and an IDC10 connector.
A□ center negative wall transformer (+9 V, 500 mA); and a PC or PC compatible computer.

The minimum software requirements are:
Microsoft C/C++ or Borland C/C++ , or Turbo C/C++ 3.0;
Paradigm DEBUG,LOCATE; and TERN System Disk including PD.LIB.

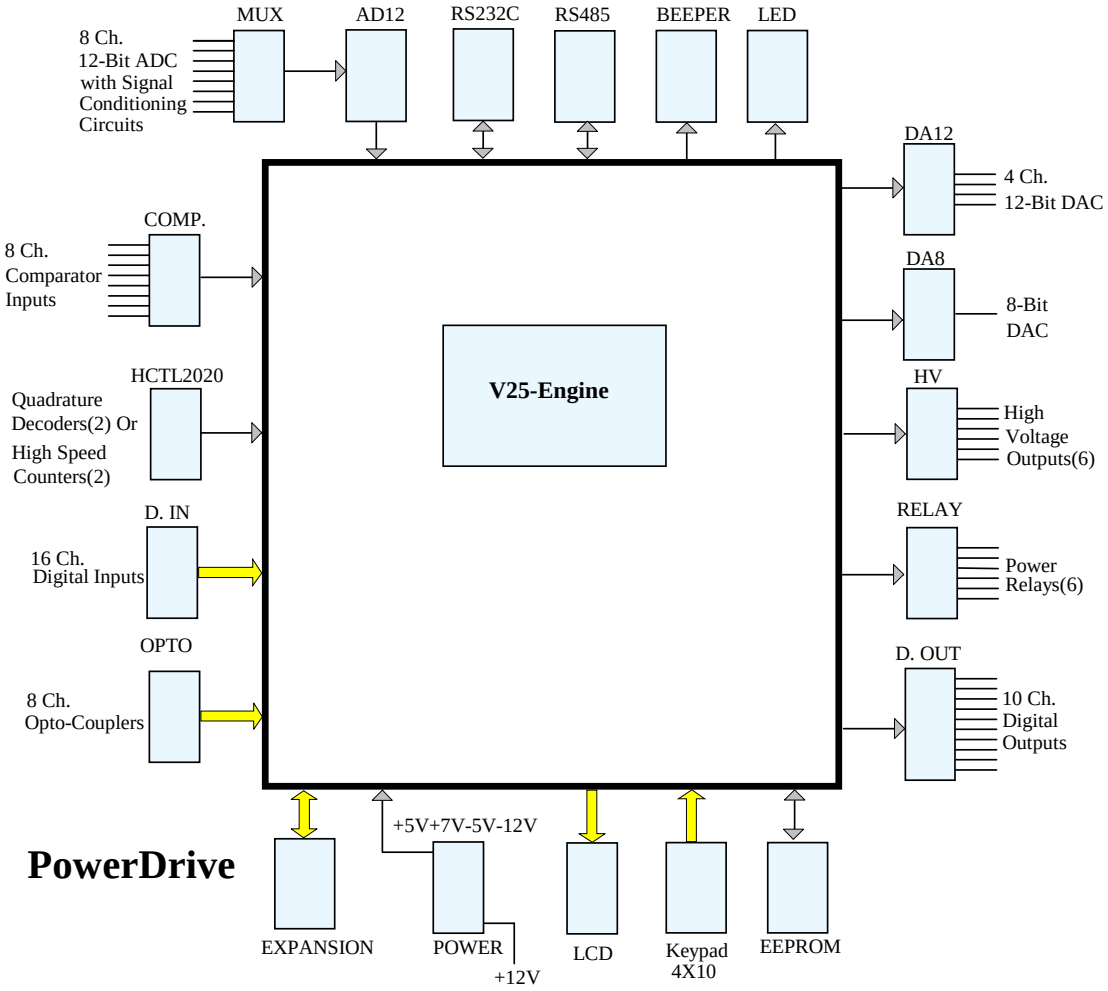


Fig. 1.1 Functional block diagram of the PowerDrive

1.3 Features

- 7.9 x 5.6 x 0.8 inch
- Power consumption: 190 mA at full speed (16MHz)
- Low power version: 50 mA standby
- 16-bit CPU (V25 NEC), 16MHz, Intel 80x86 compatible
- 32K-512K EPROM, 32K-512K SRAM
- 256 bytes built-in RAM, DMA, 5 external interrupts
- Two 16-bit timers, 16-bit time base counter
- 24 bidirectional I/O lines in the V25 CPU
- Eight V25 comparators for analog or digital inputs
- Analog MUX (DG508) and signal conditioning circuit
- Fifteen(7+8) channels of 10-bit analog inputs
- Two RS-232 serial ports and one RS-485 UART
- Real-time clock, lithium coin battery
- EEPROM 512 bytes (up to 8KB), supervisor chip (691)
- One channel 10-bit DAC output

- Six high voltage/current outputs
- Sixteen digital inputs and 10 digital outputs
- Six power relays with NO, NC and COM terminals
- Beeper, LCD, keypad and PDC interface
- 72-position terminal block and expansion port
- Eight channels 12-bit ADC
- Four channels 12-bit DAC
- Two channels quadrature decoder/counters
- Eight opto-couplers accept either AC or DC inputs

1.4 Physical Layout

Fig. 1.2 shows the physical layout of the PowerDrive. A V25-Engine micro-computer core module is the main part of the PowerDrive. T1-T4 are terminal block connectors (18x1). All small circles close to jacks or headers in Fig. 1.2 indicate the pin number 1 of the corresponding connectors.

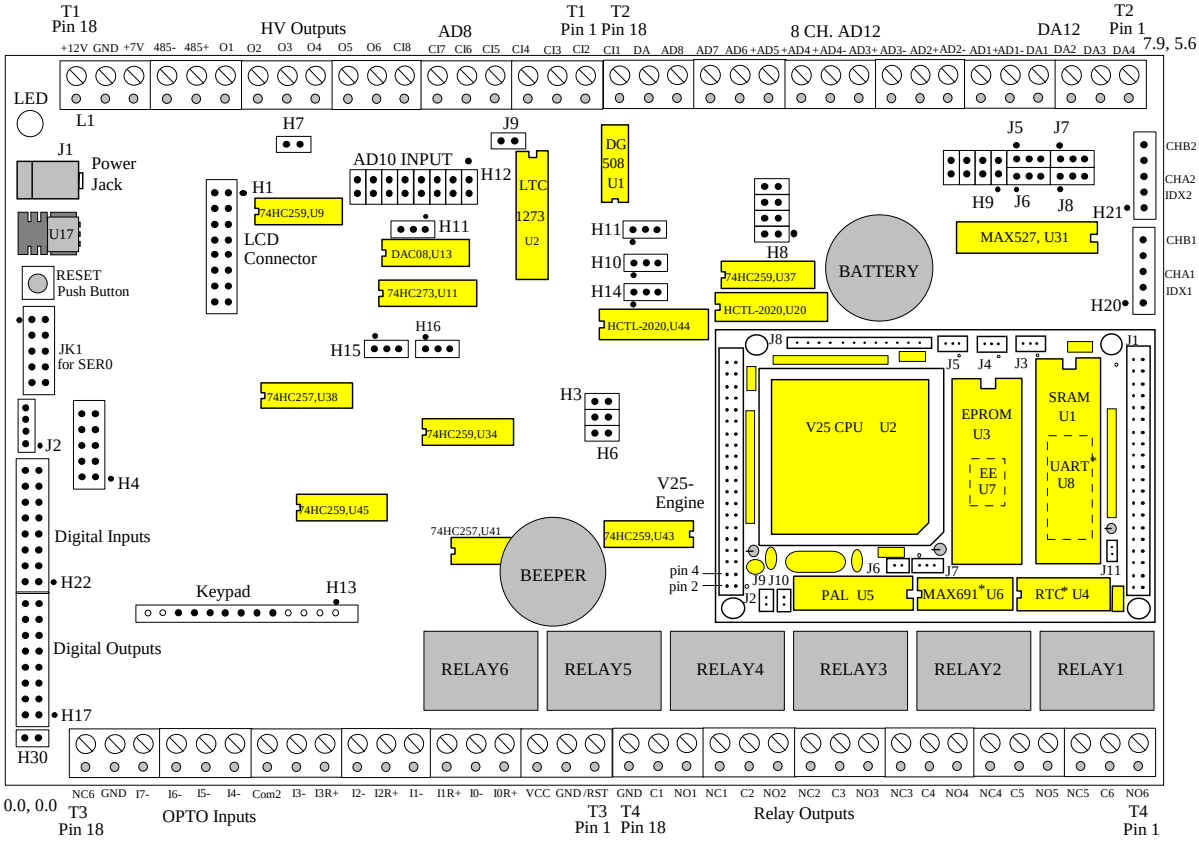


Fig. 1.2. Major components used in the PowerDrive

Chapter 2
Installation

2.1 Software Installation
See V25-Engine™ or C-Engine™ manual for software installation.

2.2 Hardware Installation
1. Connect the IDC10 connector of the RS232 serial cable to JK1 of PowerDrive™, with the red side of the cable corresponding to pin 1 of JK1 (a small circle close to JK1 indicates pin number 1), and connect DB9 connector of the serial cable to COM1 or COM2, the PC serial port, as shown in Fig. 2.1.

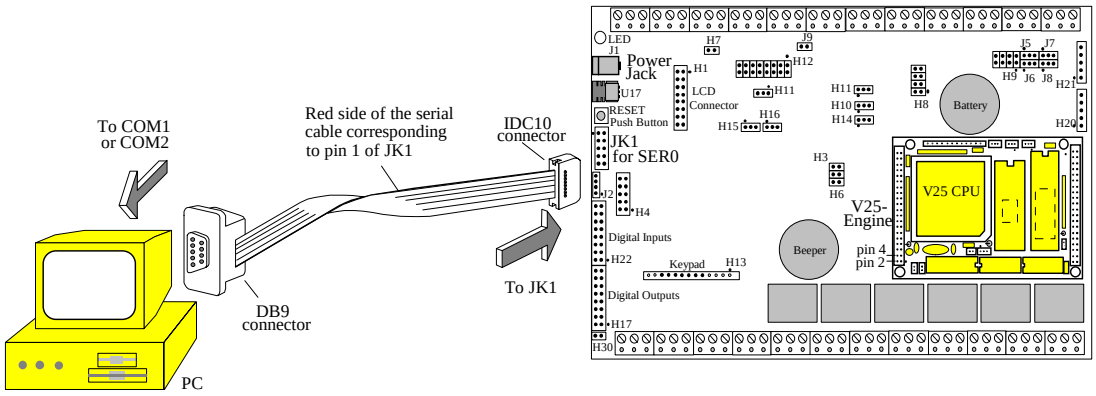


Fig. 2.1. Connection of the PowerDrive with PC

3. Connect the output of the center negative wall transformer (+9V DC) to the PowerDrive™ DC power jack J1 (Fig. 2.2).

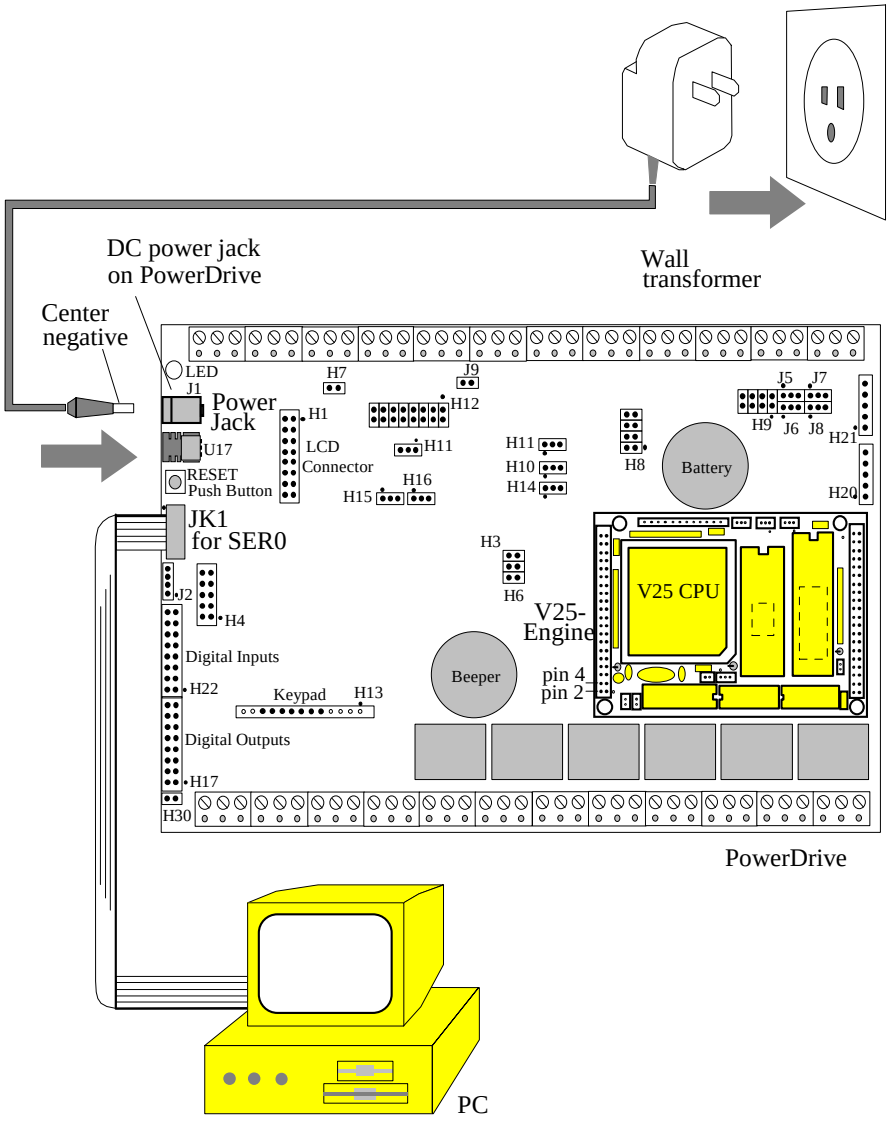


Fig. 2.2 Connection of the center-negative wall transformer to the PowerDrive™

2.3 Simple Test

You can run a simple sample program "**pd_led.c**" under your default directory "c:\samples\pd" to test the software and hardware installation. The LED on the PowerDrive™ should blink if everything is fine. The procedure involved in the test is similar to that for the simple test program "**led.c**" described in the V25-Engine™/C-Engine™ Manual.

Chapter 3
Hardware

3.1 V25-Engine™ or C-Engine™

The PowerDrive™ uses a V25-Engine™ or a C-Engine™ as its microprocessor core module. Please refer to the V25-Engine™ or C-Engine™ Technical Manual for more information.

3.2 PowerDrive I/O Map

The following tables list the I/O address of the PowerDrive™, together with their Data Bits, Chip-Select Symbol and Functions. The layout and physical locations of those devices are in Fig. 1.2.

Table 3.1. Write devices

Address	Data Bits	Chip-Select Symbol	Function
0x60	D0-7	/DAC	Write D0-7 to 74HC273 (U11), which is the input buffer for DAC08 (U13). Full scale (0-0xff) corresponds to output range 0-5V at DAC output pin
0x64	D0 as data, D1-3 as addr	/KEYH	Write D0 to one of the eight registers in 74HC259 (U34), **D3 D2 D1 Register D3 D2 D1 Register** 0 0 0 HOI1 1 0 0 HOI5 0 0 1 HOI2 1 0 1 SCL1 0 1 0 HOI3 1 1 0 DO17 0 1 1 HOI4 1 1 1 EN485 where HOI1-5 are control lines for the keypad drive, SCL1 is the clock signal for the serial EEPROM , EN485 is the chip-select signal for LTC485 (U5), and DO17 is used as /RTS1 signal to 1488 (U4) and is available at H22 pin 3.
0x68	D0 as data, D1-3 as addr	/HV	Write D0 to one of the eight registers in 74HC259 (U9), **D3 D2 D1 Register D3 D2 D1 Register** 0 0 0 DR1 1 0 0 LED 0 0 1 DR2 1 0 1 DR7 0 1 0 DR4 1 1 0 DR5 0 1 1 DR6 1 1 1 DR3 where DR1-6 are registers for high voltage/current output O1-6, LED is the signal line turning the LED on and off, and DR7 is reserved for future use.

<table>
<tr><td>0x6c</td><td>D0 as data, D1-3 as addr</td><td>/CON</td><td>Write D0 to one of the eight registers in 74HC259 (U37),
D3 D2 D1 Register D3 D2 D1 Register
0 0 0 MUX0 1 0 0 /RST1
0 0 1 MUX1 1 0 1 /RST2
0 1 0 MUX2 1 1 0 B1
0 1 1 MUEN 1 1 1 B2
where MUEN is the chip-select and MUX0-2 the address signals for MUX (U1), /RST1, /RST2 for HCTL2020 decoders (U20 and U44), and B1, B2 are reserved for future use.</td></tr>
<tr><td>0x70</td><td>D0 as data, D1-3 as addr</td><td>/OUT1</td><td>Write D0 to one of the eight registers in 74HC259 (U45),
D3 D2 D1 Register D3 D2 D1 Register
0 0 0 DO1 1 0 0 DO5
0 0 1 DO2 1 0 1 DO6
0 1 0 DO3 1 1 0 DO7
0 1 1 DO4 1 1 1 DO8</td></tr>
<tr><td>0x74</td><td>D0 as data, D1-3 as addr</td><td>/OUT2</td><td>Write D0 to one of the eight registers in 74HC259 (U43),
D3 D2 D1 Register D3 D2 D1 Register
0 0 0 DO9 1 0 0 DO13
0 0 1 DO10 1 0 1 DO14
0 1 0 DO11 1 1 0 DO15
0 1 1 DO12 1 1 1 DO16 where DO9-DO14 control relays 1-6, respectively, DO15 controls the Beep, and DO16 is available at H22 pin 1.</td></tr>
<tr><td>0x78</td><td>D0 -3</td><td>/DAMSB</td><td>Write MSB D8-D11 to the 12-bit DAC MAX527 (U31).</td></tr>
<tr><td>0x7c</td><td>D0-7</td><td>/DALSB</td><td>Write LSB D0-D7 to the 12-bit DAC MAX527 (U31).</td></tr>
<tr><td>0x080</td><td>D0-7</td><td>LCD1</td><td>Write D0-7 to LCD1 (H1)</td></tr>
<tr><td>0x0a0</td><td>D0-7</td><td>LCD2</td><td>Write D0-7 to LCD2 (H1)</td></tr>
</table>

Table 3.2 Read Devices

Address	Data Bits	Chip-Select Symbol	Function
0x60 0x61	D0-D7	/ADC	Reads data from the 12-bit ADC (U2). Inportb (0x60) reads the low byte D0-D7 data, and inportb (0x61) reads the MSB D8-D11.
0x68 0x69	D0-D7	/CI	D4-D7 are read from the quadruple 2-to-1 selector 74HC257 (U38) and D0-D3 from 74HC257 (U41). The address 0x68 selects the "A" inputs and 0x69 selects the "B" inputs. D0 D1 D2 D3 D4 D5 D6 D7 "A" V1 V3 V8 V6 U42A U36A U36B U42B "B" V2 V4 V7 V5 U42D U36D U36C U42C where U42 and U36 are comparator LM339's, and V1-V8 are the vertical lines of the keypad (H13).
0x6c 0x6d	D0-D7	/INS	D4-D7 are read from 74HC257 (U22) and D0-D3 from 74HC257 (U46). U22 selects signals used by other components and U46 selects the opto-coupler inputs. The addres 0x6c selects the "A" inputs and 0x6d selects the "B" inputs. D0 D1 D2 D3 D4 D5 D6 D7 "A" I5A I6A I7A I8A HO5 IDX2 U/D2 U/D1 "B" I5B I6B I7B I8B IDX1 /INT1 /BSY PR where IxA and IxB are outputs of the opto-couplers ps2506's (U51 and U52); HO5 is the horizontal line 5 of the keypad (H13); U/D1 and U/D2 are upper or down signals of HCTL2020's (U20 and U44); /INT1 reads CAS, the overflow /underflow signal from U20 when H10 pins 1 and 2 are connected (U44 's CAS signal CAS2 is not readable but is connected to /INT2 to generate interrupts when H14 pins 1 and 2 are connected by a jumper); /BSY is a busy signal of the 12-bit ADC LTC1272 (U2); IDX1/IDX2 is the input from the index pulse of some optical encoders, which is generated once per full rotation of the codewheel; PR is a status bit for a configuration jumper at H6.
0x70	D0-D7	/IN1	Reads H22 digital inputs.
0x74		/LDAC	Inportb(0x74) transfers the contents of each of the four input registers to its respective DAC register of 12-bit DAC data into voltage output stage.
0x78 0x79	D0-D7	/HP1	Inportb(0x78) reads the high byte of the results from HCTL2020 (U20), and inportb(0x79) reads the low byte.
0x7c 0x7d	D0-D7	/HP2	Inportb(0x7c) reads the high byte of the results from HCTL2020 (U44), and inportb(0x7d) reads the low byte.
0x80-9f	D0-D7	LCD1	Reads H1 D0-D7.
0xa0-bf	D0-D7	LCD2	Reads H1 D0-D7.

3.4 12-Bit Analog Input Channels (8)

The 12-bit analog input channels (8) consist of a signal conditioning stage (8 channels), a multiplexer, and a 12-bit ADC. The multiplexer selects one of the eight analog input channels at one time, and the signal conditioning stage provides adequate signal conditioning including preamplifying and filtering.

Multiplexer

An 8-to-1 analog multiplexer (HI-508A or DG508A, Fig. 3.1) selects one of the 8 analog input channels according to control signal MUX0-2 and the enable signal MUEN = 1. The output signal of the multiplexer is ADI, which is buffered by an op-amp (U54, OP07). The gain of this op-amp is calculated according to (1 + R51/R50) (R50 and R51 are resistors used by U54, see Fig. 3.1). R51 has a default value of 200Ω, and R50 a value of 20 KΩ, therefore the default gain is approximately 1. Changing R51 changes the gain. AIN, the output signal of the op-amp, is connected to the input of a 12-bit ADC (LTC1272, U2) or one of the channels of the comparator inputs (CI1) by setting a jumper on J9. The typical on-resistance of the multiplexer is 1.5 KΩ.

When MUEN = 0, the multiplexer is disabled, and the analog signals are isolated from the ADC.

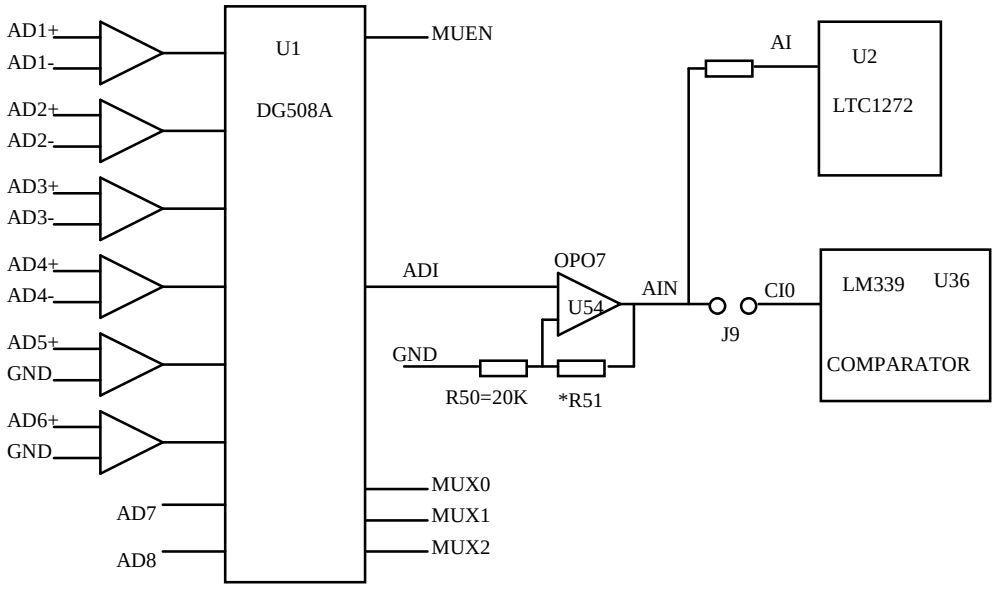


Fig. 3.1. The multiplexer selects one of the eight analog input channels

3.4.2 Signal Conditioning

Four differential op-amps (Fig. 3.2) and two non-inverting op-amps (Fig. 3.3) with configurable gains and filters constitute a preamplifier stage for the 12-bit analog input channels. A pull-up resistor network (RN9) may be installed to provide +7V DC power supply for some sensors. Channel 1 to channel 4 are differential op-amp channels with optional low-pass filters. The gains of these channels in the passband (approximated by the ratio of RP3/RP1 or RP5/RP2, see Fig. 3.2,) can be configured by changing the value of RP3 or RP5 (RP1 and RP2 are fixed). By default, RP3 = RP5 = RP1 = RP2 = 10K, and R51=0. Gain≈ 1. Capacitors C4-C7 are set by users, and the cutoff frequency can be estimated according to 1/(2πRPxCx), with RPx = RP3 or RP5, and Cx = C4 to C7.

Channel 5 and 6 use non inverting op-amps with the pass band gains ≈ RP7/RP6. The user can set different gains by using different RP7 values. By default, RP6 = RP7 = 10K, and the pass band gain ≈ 1. The cutoff frequency of the lowpass filters are estimated according to 1/(2πRP7Cx) with Cx = C54 or C55. Channels 7 and 8 are connected to the multiplexer directly(Fig. 3.3).

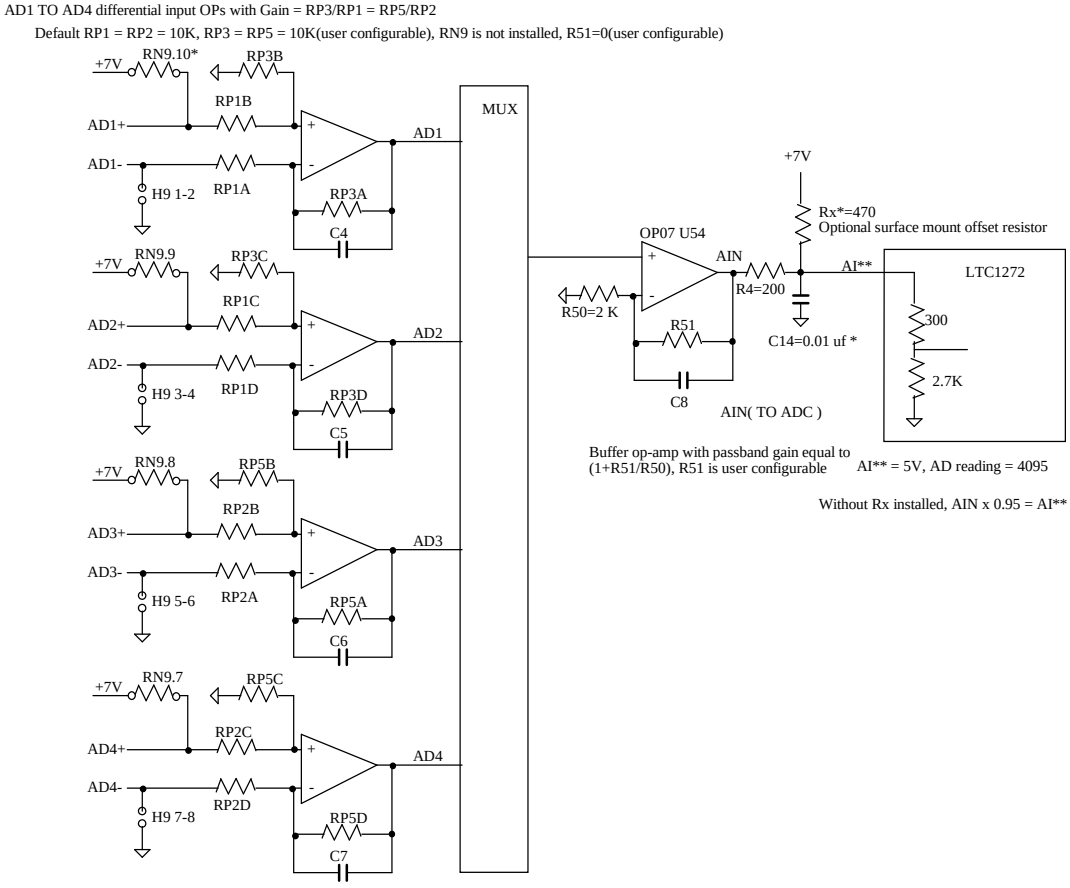


Fig. 3.2. Signal conditioning stage, four differential op-amps

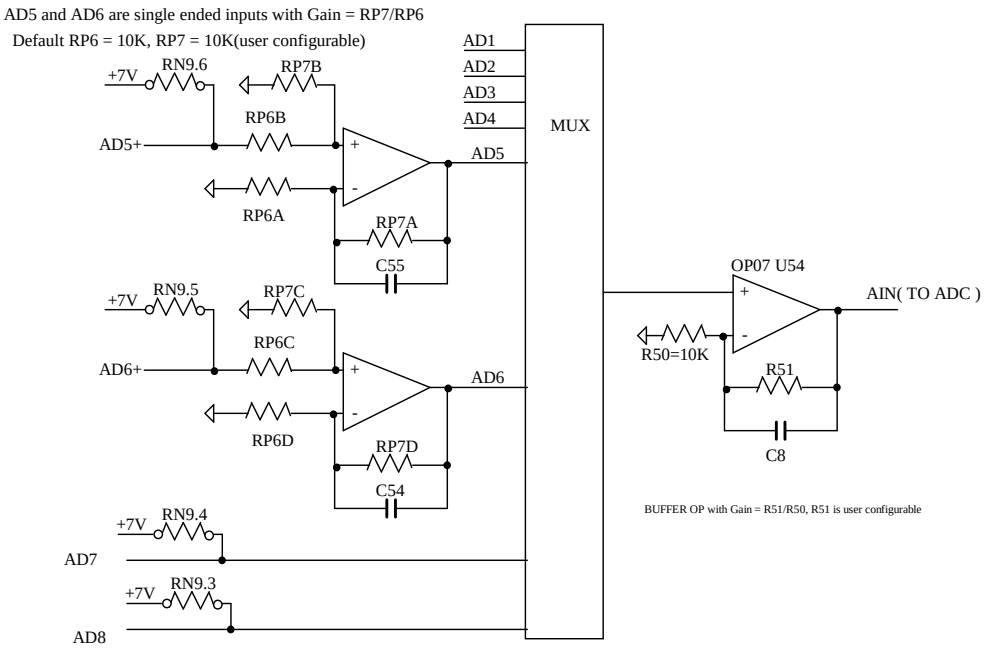


Fig. 3.3. Signal conditioning stage, two non inverting op-amps

3.4.3 12-Bit ADC

A 12-bit ADC (LTC1272-3/5/8, Linear Technology) is used to accept the output from the U54 Op and the multiplexer. The LTC1272 is a 3/5/8-µs, 250-kHz sample rate, 12-bit, successive approximation sampling A/D converter. It has the same pinout as the industry standard AD7572 and offers faster conversion time, on-chip sample-and-hold, and single power supply operation. The LTC1272 has an internal reference voltage (2.42 V) which is also used by the 12-bit DAC on the PowerDrive™. LTC1273/1275/1282 are pin compatible ADCs with different specifications.

The LTC1272 connects AIN input to the sample-and-hold capacitor through an internal 300Ω/2.7K resistor divider. This divider plus the external R4=200Ω, allows the LTC1272 to convert 0V to 7V input signals. Corresponding to the analog input voltage at pin 1 of LTC1272, the output code is natural binary with 1LSB=FS/4096=5/4096=1.22 mV. The voltage drop at R4 will cause approximately AIN x 95% = AI**, see Fig. 3.2. A simple calibration procedure can be used to calibrate the error of the signal conditioning circuit. The factory default setting is: while Adx- = GND, Adx+ = 5.25V input voltage at the screw terminal, the AD reading is approximately at full counts, 4095. User may install different values of gain resistors in the machine hole sockets to set the required gain for the application.

When the analog input voltage is taken below ground, it will be clamped by an internal diode of LTC1272. It can handle, with no external diode, input currents of greater than 60 mA below ground without latch-up. In order to prevent the analog input signal below ground, an offset summing resistor Rx=470Ω may be added to the AI pin 1 of LTC1272, as shown in Fig. 3.2. Rx may be a surface mount resistor found on the solder side of PowerDrive board. You may solder connect it to the +7V as shown in Fig. 3.3a. The Rx resistor will offset the analog input at pin 1 of LTC1272 to 2.5V while the U54 Op. output is zero volt approximately While the U54 Op output is negative 3.5V, the analog input at pin 1 of LTC1272 can be zero volt. The Rx is not installed as default. For bi-polar application, you may use LTC1275.

The I/O address for the LTC1272 is 0x60 and 0x61 (Table 3.2). A function, ***pd_ad12()***, is available in the PD. LIB for reading the ADC. The multiplexer control ***pd_mux_en***(char en); and ***pd_mux***(char ch); must be used to enable and select analog input signal before using ***pd_ad12***();.

3.5 12-Bit DAC

MAX527A provides four channels of 12-bit voltage-output (unipolar mode, analog output range: 0-5 V). Each channel has double-buffered interface logic with a 12-bit input register and a 12-bit DAC register. Data are loaded into the input register using two write operations with an 8-bit LSB and a 4-bit MSB write load. An asynchronous load DAC (/LDAC) input signal transfers data from the input register to the DAC register. Data in the DAC register sets the DAC output voltage. Precision output buffer amplifiers are included on-chip. The MAX527A operates with ±5V power supplies. You can operate the 12-bit DAC with *pd_da12*(char ch, int dat); where ch = 1-4, dat=0-4095.

3.6 10-Bit DAC

An 10-bit high-speed DAC (DAC08, U13, Fig. 3.4) with voltage/current outputs is available. J11 selects the voltage or current output. With J11 pin 1 and pin 2 connected, the DAC outputs a current (0-20 mA) at the terminal block T2 pin 17 corresponding to the digital input (0-1023).

With J11 pin 2 and pin 3 connected, a voltage (0-5 V) is output at T2 pin 17 corresponding to the digital input (0-1023). A software function ***pd_da10*** *(dat)* is available in PD.LIB.

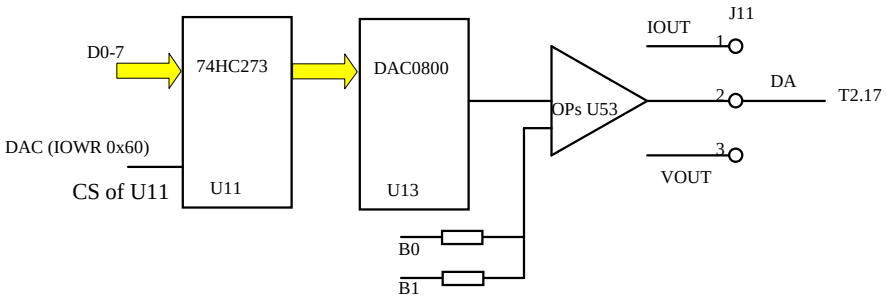


Fig. 3.4. The DAC10 channel

3.7 Comparator Inputs

There are eight channels of voltage comparator (LM339, U36 and U42) inputs on the PowerDrive™. The user can use these comparator inputs at the terminal block T1 pin 1-7 and T2 (Fig. 1.2). An additional low-cost 8-bit ADC can be constructed using these low-cost precision comparators and the 8-bit DAC on the PowerDrive™. The DAC08 output may be connected to one of the comparator inputs. To detect the analog input signal voltage level at another input pin, the DAC08 needs to be programmed to step up or down the output, which acts as a variable reference voltage on the comparator input. If the DAC output voltage is lower than the analog signal input, the comparator output 1, and this bit value is recorded. Otherwise, the comparator outputs 0, which is also recorded. All the bit-values recorded form a value corresponding to the measured analog signal level. The reference voltage, DAV, of the comparator can also be set to a fixed voltage level RR, which is the output of a resistor divider (R27 and R33). H16 is used to set DAV value to that of DA (connecting H16 pins 2-3) or to that of RR (connecting H16 pins 1-2). A block diagram of the comparator circuits is shown in Fig. 3.5. A function ***pd_ad10(****int* ad****)*** reads the ADC and puts readings into an integer array.

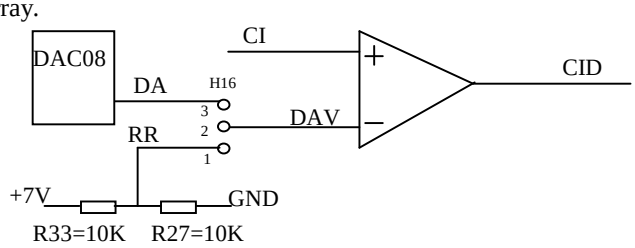


Fig. 3.5. Comparator inputs

3.8 Opto-Couplers

The opto-coupler is an optically coupled logic gate that combines an LED and a photon detector. The output of an opto-coupler can be interfaced to the microprocessor digital circuit, while the LED input can be connected to a high voltage signal line. It is frequently used to prevent a microprocessor system from being interfered by voltage transients on a signal line or isolate a microprocessor system from high voltage inputs. On the PowerDrive™ the opto-couplers are used for isolation of the high voltage inputs from the microcomputer system. Eight channels of opto-couplers (PS2506, NEC) are available at the terminal blocks T3 pin 4-16. The opto-coupler input channels 0-3 have independent positive inputs (IxR+) and negative inputs (IxR-) (Fig. 3.6). The user must provide both IxR+ and IxR- to channel 0-3. The opto-coupler channels 4-7 use a common positive input Com2 (at T3 pin 12, Fig. 1.2) and individual negative inputs I4-, I5-, I6- and I7- (at T3 pins 13-16, Fig. 1.2). 4.3-K resistors are used to limit the input current to the LED in the opto-coupler.

3.9 HCTL2020

Two quadrature decoder/counter interface chips, (HCTL2020, Hewlett Packard, U20 and U44) are included on the PowerDrive™. The quadrature decoder is used to interface incremental motion encoders with the microprocessor system or to improve system performance for digital close-loop motion control systems. The HCTL2020 includes a quadrature decoder, a 16-bit counter, and an 8-bit bus interface. It features full 4x decoding, 14-MHz clock operation, high noise immunity due to the use of schmitt trigger inputs and digital noise filters, quadrature decoder output signals, up/down signal, count signals, and cascade output signal. Many types of optical incremental encoder modules, such as HEDS-9000, HEDS-9100, and HEDS-9200 from HP, can be directly interfaced to the HCTL2020. Channel A, B, and index pulse signal from some optical encoders (CHAx, CHBx, IDXx, with x = 1 or 2) are input at pins 3, 5, and 2 on headers H20 and H21 of the PowerDrive™ (Fig. 1.2). All inputs to the HCTL2020 are buffered by Schmitt triggers (74HC14, U39, fig. 3.7). The HCTL2020 has built-in filters which allow reliable operation in noisy environment. The PowerDrive also provides an option for the HCTL2020 to be used as a high speed digital counter, if the function of the quadrature decoder is not used. When H8 pins 1-2 (or pins 5-6) are connected, U20 (or U44) is used as a quadrature decoder, with its inputs being CHA1 and

CHB1 (or CHA2 and CHB2). When H8 pins 3-4 (or pins 7-8) are connected, U20 (or U44) is used as a 16-bit counter for counting high-speed digital inputs on CHA1 (or CHA2). Two functions are available to operate the quadrature decoders: unsigned int ***pd_hp_rd***(char ch); and void ***pd_hp_reset***(char ch);

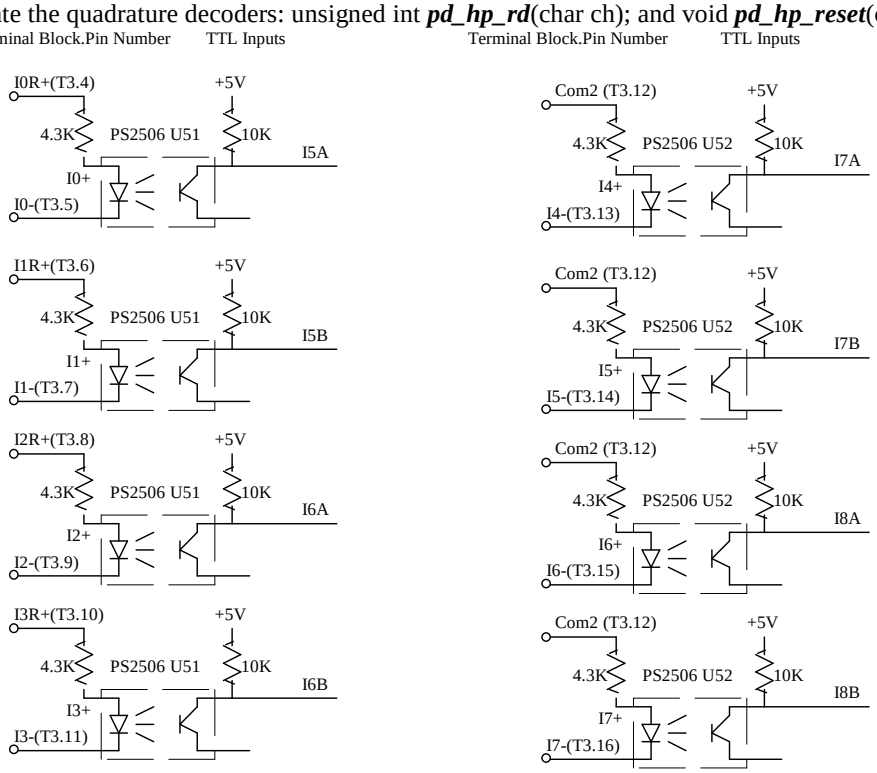


Fig. 3.6. Eight opto-coupler input channels.

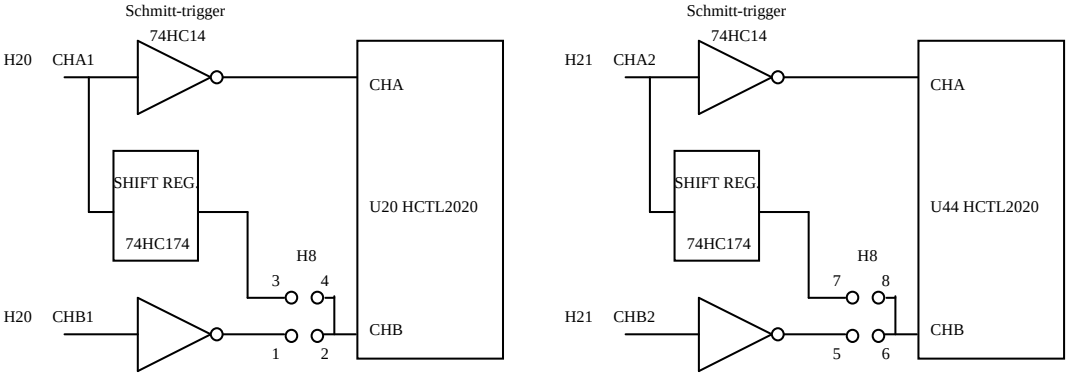


Fig. 3.7. Quadrature decoders for motion detection, or high speed counters

3.10 Keypad

H13 on the PowerDrive™ is a 13-pin header for interfacing with a matrix keypad. It can support upto 5x8 = 40 keys. HO1-5 are horizontal control lines and V1-8 the vertical input lines of the keypad. You may use int ***pd_kb_scan*** (void); to read keycodes. The V1 to V8 lines are pulled high with on board 10K resistors. You may read in D0-D3 for the V1-8 from the 74HC257 U41 with ***inportb***(0x68); and ***inportb***(0x69);. See Schematics and Table 3.2 for details. You may set all HO1-5 high first, then set one line low at one time for scan. If any key is pressed, one of the V1 to V8 lines will be pulled low by one of the HO1-5 line. You may decode the key from the HO1-5 and V1-8 information. A sample keypads application is shown in Fig. 3.8a.

3.11 LCD

H1 on the PowerDrive™ is a 2x8 header for interfacing with a 16x2 character LCD (M1632, Seiko) or a 40x8 character LCD (M4024, Seiko). Functions are available in LCD.LIB.

3.12 Beeper and LED

The beeper and the LED on the PowerDrive™ can be controlled with software functions:
void ***pd_beep*** (int,int); and void ***pd_led*** (int);

3.13 Use of the 74HC259 8-bit addressable latches

Five 74HC259 8-bit addressable latches (U9, U34, U37, U43, U45) are used for general purpose digital output (see Table 3.1). They are used for driving the keypad, EEPROM SCL1 signal, EN485 signal (U34); high voltage/current output; LED (U9); MUX selection signal, /RST1 and /RST2 for the HCTL2020; DO1-8 for the digital output at header H17; relays and the beeper control (U43). The detailed latch address is listed in Table 3.1. D1-3 of the V25 data bus are used to select one of the eight addressable latches in 74HC259, and D0 of the data bus writes the data D0 into the latch selected by D1-D3 .
For examples, ***outportb*** **(**0x68, 0x09**)** will turn the LED off and ***outportb*****(**0x68, 0x08**)** will turn the LED on, where 0x68 is the address of 74HC259 and 0x8 is the address of the latch for the LED.

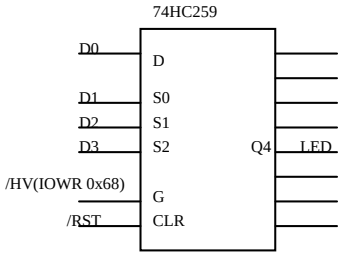


Fig. 3.8. Use of 74HC259, the addressable latch

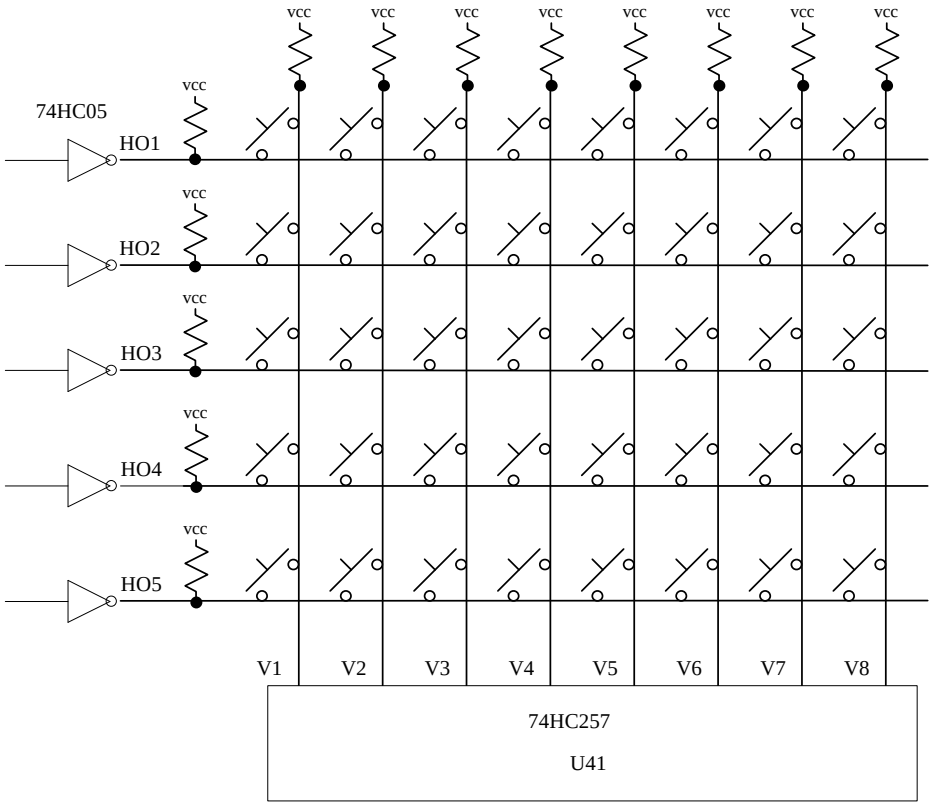


Fig. 3.8a. A sample keypads application.

3.14 Digital inputs

Eight channels of TTL digital inputs are connected to H22, a 8x2 header (H22 is located at the left lower corner of Fig. 1.2), as shown in Fig. 3.9. These inputs can be read at I/O address 0x70 and 0x71 by calling ***inportb*** function or the function of *int* ***pd_di***(void);. It returns an integer with a low byte with status of H22 I1a=bit 0, I2a=bit 1, I3a=bit 2, I4a=bit 3, I1b=bit 4, I2b=bit5, I3b=bit6, I4b=bit7

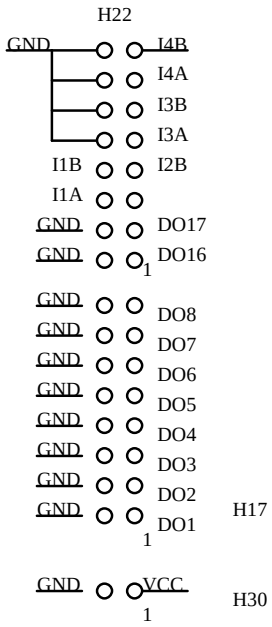


Fig. 3.9 Digital inputs and outputs at H22.

3.15 Digital Outputs

Eight channels of TTL digital signal outputs DO1-8 are available on H17 (located at the left lower corner of Fig. 1.2). DO16 and DO17 are on H22 (pin 1 and pin 3, Fig. 3.9.). You may use ***pd_dout***(int p, int s) to control DO1-8. For example, to control DO3 pin output high/low, use ***pd_dout***(3, 1); / ***pd_dout***(3,0);.

The digital outputs on H17 use the 74HC259 addressable latches (U45) to store the data. DO1-DO8 also may be controlled by calling the routine ***outportb***(addr, data), where addr = 0x70 (See Table 3.1 for more details). For DO16, addr = 0x74 and data = 0x0f or 0x0e. For DO17, addr = 0x64 and data = 0x0d or 0x0c. DO17 is also used as /RTS1 signal for 1488 (U4).

3.16 Power Relays

The PowerDrive™ supports upto six power relays. The normally open pin, normally close pin and common pin of the power relays are connected to the terminal blocks with heavy trace, supporting at least 5A current. They are also controlled by calling ***outportb*** (addr, data), where addr = 0x74, data = 0x00 to 0x05. You may use the function:

void ***pd_relay***(int r, int s); where r=1 to 6 for 6 power relays, and s=1/0 for relay on/off.

3.17 RS232C and RS485

The V25 internal serial channel 0 (SER0) and serial channel 1 (SER1) are supported with RS232C drivers. The SER0 signals are on the phone jack (JK1) or the 2 x 5 header (JK2). The SER1 signals are on H4. SER1 can be connected to RS232 driver or RS485 driver. The 485+ and 485- signals can be accessed on the terminal blocks T1 pin 14 and pin15.

3.18 High-voltage, High-current Drivers

ULN2003 has high voltage, high current Darlington transistor arrays, consisting of 7 silicon NPN Darlington pairs on a common monolithic substrate. All channels feature open-collector outputs for sinking 350 mA at 50V, and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA sinking are allowed. The outputs may be paralleled to achieve high-load capability, although each driver has a maximum continuous collector current rating of 350 mA at 50V. The maximum power dissipation allowed is 2.20 W per chip at 25 degree C. The common substrate G is routed to T2 pin 17 GND. All currents sinking in must be return from T2 GND pin. A heavy gage(20) wire must be used to connect T2 GND terminal to external power supply ground return. K is connecting to the protection

diodes. K should be tied to highest voltage in the external load system. It has been connected to +12V on board via H7. ULN2003 is a sink driver, not a sourcing driver. A typical application wiring is shown in Fig. 3.10

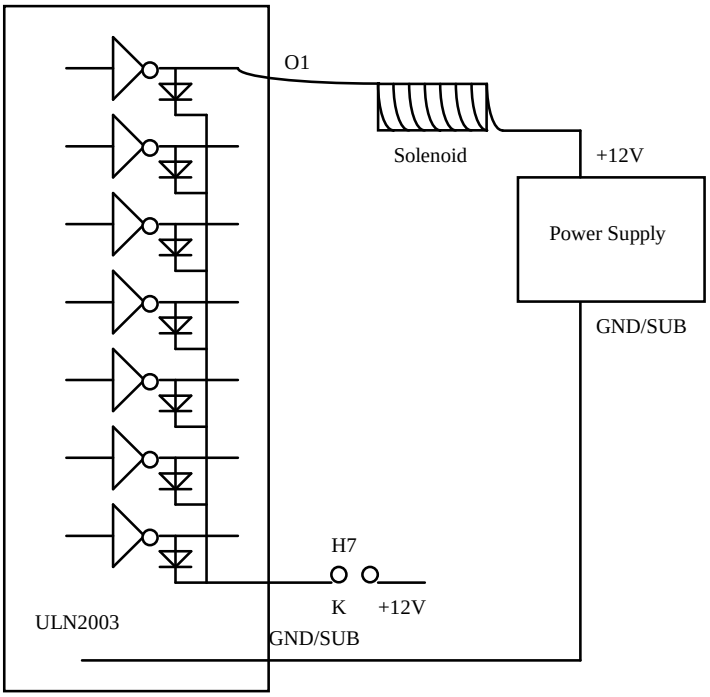


Fig. 3.10 Drive inductive load with high voltage/current drives.

Chapter 4
Software

Please refer to the C-Engine™ Technical Manual for more details.

Functions in PD.LIB Library

int pd_kb_scan (void); scan keypad to identify which key is pressed
Return: 0FFh if no key is detected
1-0x0c if key is detected, 1 for top-left key, 12 for lower-right key,
with TKA2200 4x3 Telephone Keypad LZR 301-921-9440

void pd_beep (int l, int f); Sounds the beeper with time length of "l" at frequency of "f".
Try pd_beep(200, 30);

void pd_led (int); On board LED control. pd_led(1) turns on the LED.

void pd_relay(int r, int s); Power relay control. pd_relay(3, 1); will turn relay 3 on.
where r=1-6, s=0/1.

void pd_da10(int dat); Output analog voltage at DA pin. where dat=0-1023 for 0-5V output

void pd_da12(char ch, int dat); Output 0-5V at DA1-4 for the 12-bit DAC. where ch = 1-4, dat=0-4095

void pd_mux_en(char en); Enable/disable 8-1 multiplexer. where en=1/0

void pd_mux(char ch); Select one of the eight analog inputs. where ch=1-8.

int pd_ad12(void); Return the 12-bit ADC reading of the LTC1273 12-bit ADC.
User should enable the multiplexer and select on of the eight analog inputs before using this function.

unsigned int pd_hp_rd(char ch); Returns the 16-bit HP2020 quadrature encoder reading. where ch=0/1

void pd_hp_reset(char ch); Reset the HP2020. where ch=0/1 for channel 0 or 1

void pd_ad10(int* ad); Return the 8 channels of comparator analog input reading in int* ad.
Use the on-board 10-bit DAC for reference.

void pd_hv(int ch, int k); Control high voltage drivers O1-6. where ch=1-6, k=0/1 for low/high

int pd_opto(int ch); Returns the status of the eight channel Opto-coupler inputs.
where ch=0-7. If returns 0, the "ch" opto-coupler is ON

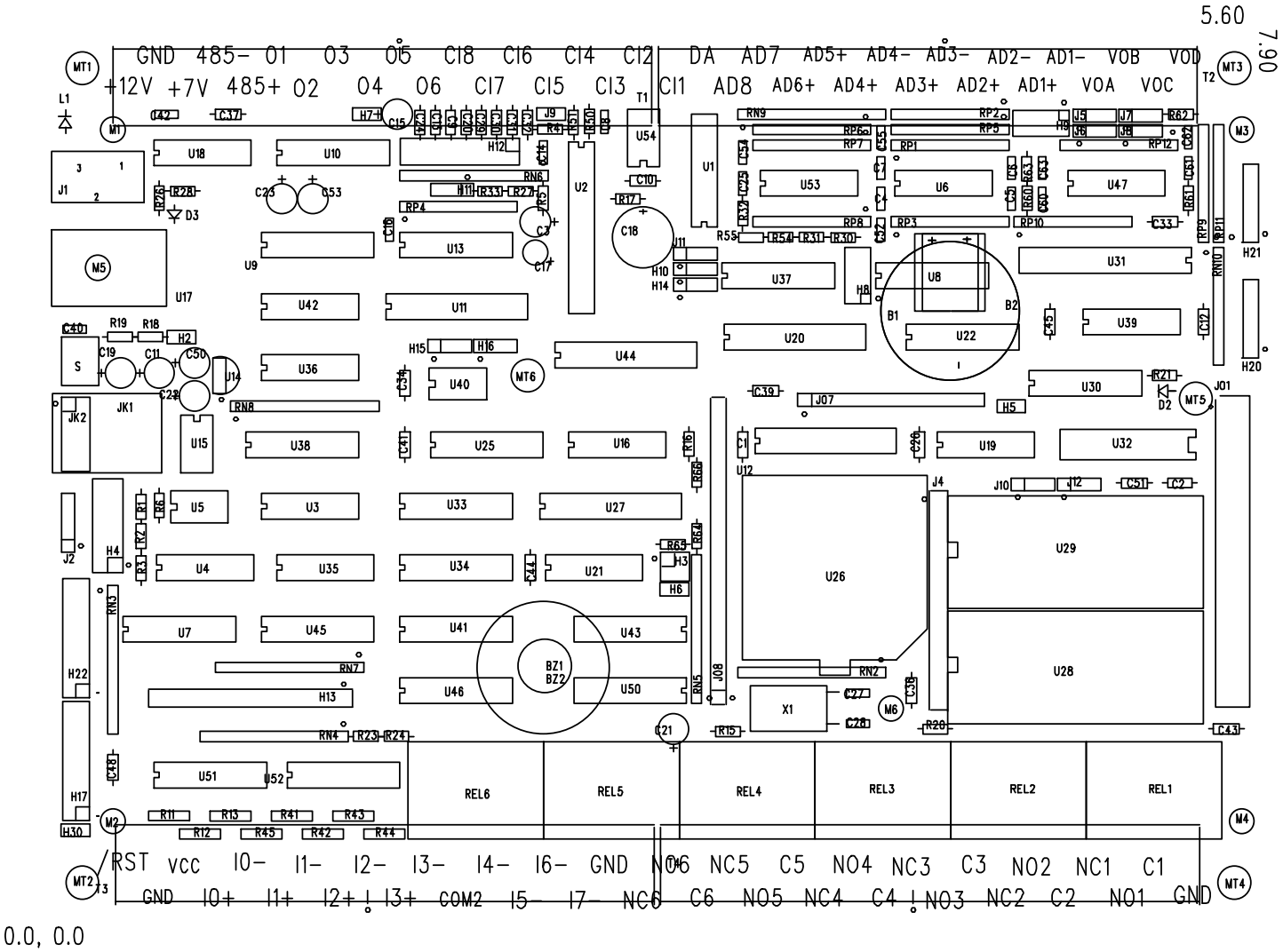
int pd_di(void); Returns a low byte of 8-bit status of digital inputs on H22.
I1a=bit 0, I2a=bit 1, I3a=bit 2, I4a=bit 3, I1b=bit 4, I2b=bit5, I3b=bit6, I4b=bit7

void pd_dout(int d, int s); Output s to digital output Do1-Do8 on H17.

int pd_ee_rd(int address); Reads one byte from external EEPROM memory location of address.

int pd_ee_wr(int address, char datum); Writes datum to external EEPROM at location of address

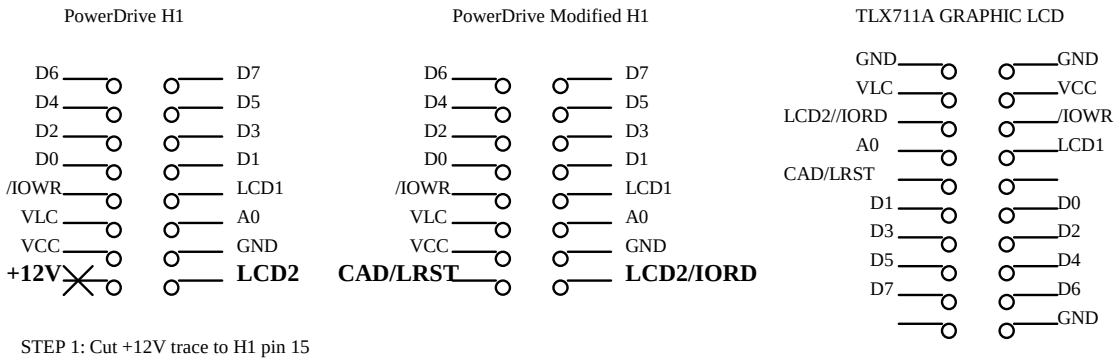
Appendix A: PowerDrive™ Layout



Appendix B: How to interface a graphic LCD(TLX711A/UG-24B-03GNBR) to the PowerDrive™.

The PowerDrive™ LCD interface H1 is a 16 pin header designed for interfacing to character type LCD directly. The H1 pin functions and the graphics LCD header functions are shown in the Fig. below.

This is the view at the component side of PCB
H1 on the Schematics is the mirror of layout on PCB

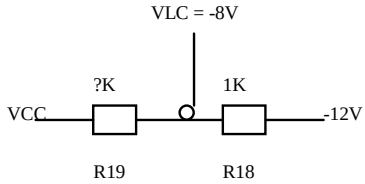


STEP 1: Cut +12V trace to H1 pin 15

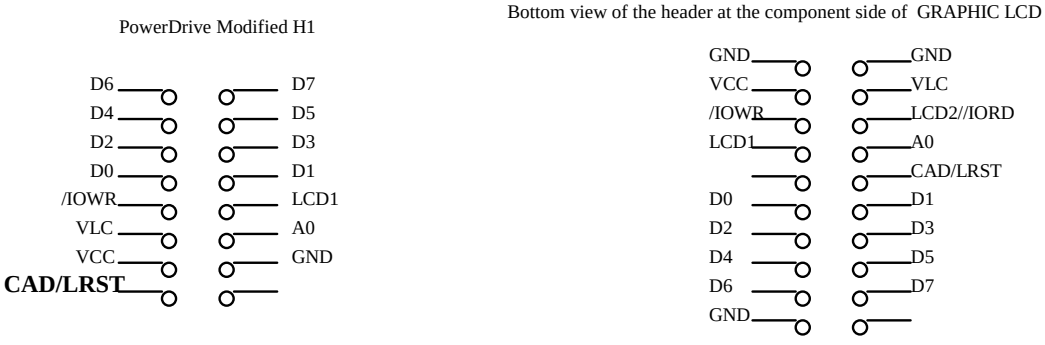
STEP 2: Use PAL PDP010 in U27

STEP 3: Add a wire between H14.2 to H1 pin 15

STEP 4: Provide correct VLC=-8.20 V to VLC with R18 and R19. (R18+R19=10K)



STEP 5: Use PD_GLCD cable



If the on-board negative power supply is not capable to provide negative voltage for ADC, OPs, RS232 drivers and the graphic LCD VLC, use external negative adjustable power supply for VLC.

Appendix C: PowerDrive I/O Map

CPU Internal I/O registers Address	Name	Description
00	CNTLA0	Serial Ch 0 control register A
01	CNTLA1	Serial Ch 1 control register A
02	CNTLB0	Serial Ch 0 control register B
03	CNTLB1	Serial Ch 1 control register B
04	STAT0	Serial Ch 0 status register
05	STAT1	Serial Ch 1 status register
06	TDR0	Serial Ch 0 transmit data register
07	TDR1	Serial Ch 1 transmit data register
08	RDR0	Serial Ch 0 receive data register
09	RDR1	Serial Ch 1 receive data register
0A	CNTR	Clocked serial control register
0B	TRDR	Clocked serial data register
0C	TMDR0L	Timer data reg Ch 0, least
0D	TMDR0H	Timer data reg Ch 0, most
0E	RLDR0L	Timer reload reg Ch 0, least
0F	RLDR0H	Timer reload reg Ch 0, most
10	TCR	Timer control register
11–13	—	*reserved*
14	TMDR1L	Timer data reg Ch 1, least
15	TMDR1H	Timer data reg Ch 1, most
16	RLDR1L	Timer reload reg Ch 1, least
17	RLDR1H	Timer reload reg Ch 1, most
18	FRC	Free running counter
19–1F	—	reserved registers
20	SAR0L	DMA source address Ch 0, least
21	SAR0H	DMA " " " most
22	SAR0B	DMA " " " extra bits
23	DAR0L	DMA dest address Ch 0, least
24	DAR0H	DMA " " " most
25	DAR0B	DMA " " " extra bits
26	BCR0L	DMA byte count reg Ch 0, least
27	BCR0H	DMA " " " " most

28	MAR1L	DMA mem address reg Ch 1, least
29	MAR1H	DMA " " " " most
2A	MAR1B	DMA " " " " extra bits
2B	IAR1L	DMA I/O address reg ch 1, least
2C	IAR1H	DMA " " " " most
2D	—	*reserved*
2E	BCR1L	DMA byte count reg Ch 1, least
2F	BCR1H	DMA " " " " most
30	DSTAT	DMA status register
31	DMODE	DMA mode register
32	DCNTL	DMA / WAIT control register
33	IL	Interrupt vector low register
34	ITC	Interrupt / Trap control register
35	—	*reserved*
36	RCR	Refresh control register
37	—	*reserved*
38	CBR	MMU common base register
39	BBR	MMU bank base reg
3A	CBAR	MMU common/ bank area register
3B–3D	—	*reserved*
3E	OMCR	operation mode control register
3F	ICR	I/O control register

External I/O address :

Write Registers

Address	Data bits	Symbol	Function
0x60	D0-7	/DAC	Write D0-7 to U11 74HC273 and U13 DAC08. Full scale 0xff output +5V at DA pin
0x64	D0 as data, D1-3 as addr	/KEYH	Write D0 to U34 74HC259. Keypad drive HOI1-5, Key SCL1 and EN485
0x68	D0 as data, D1-3 as addr	/HV	Write D0 to U9 74HC259. High voltage/current output O1-6. Write 0x08 to /HV for LED on, 0x09 for LED off
0x6c	D0 as data, D1-3 as addr	/CON	Write D0 to U37 74HC259. Select U1 MUX, RST1, RST2 for HP decoder and B1, B2 for DAC08 the least bits.
0x70	D0 as data, D1-3 as addr	/OUT1	Write D0 to U45 74HC259, for DO1-8 at H17
0x74	D0 as data, D1-3 as addr	/OUT2	Write D0 to U43 74HC259, Relays and Beep control
0x78	D0 -3	/DAMSB	Write MSB to 12 bit DAC U31 MAX527 (as D8-D11) .
0x7c	D0-7	/DALSB	Write LSB to 12 bit DAC U31 MAX527 (as D0-7).
0x080	D0-7	LCD1	Write D0-7 to LCD1 (H1)
0x0a0	D0-7	LCD2	Write D0-7 to LCD2 (H1)
0x0200	D0-7	/IO1	Write D0-7 to /IO1(J08). For Input/Output expansion
0x0280	D0-7	/IO2	Write D0-7 to /IO2(J08). For Input/Output expansion
0x04000	D0-3	/TIMER	Write RTC72421 registers
0x06000	D0	SCL	Write D0 to SCL of U40 EEPROM clock
0x08000	D0	/SDAO	Write D0 to SDA of U40 EEPROM data
0x0c000	N/A	HWD	Write Operation to Hit WatchDog

Read Registers

Address	Data bits	Symbol	Function
0x60	D0-D7	/ADC	Reads U2 12 bit ADC data. Inport(0x60) reads low byte D0-D7 AD data, Inport(0x61) reads high byte D8-11 AD data.
0x68	D0-D7	/UI	Reads U38 (D4-7)and U41 (D0-3) data. U41 inputs H13 Keypads vertical inputs(V1-V8). U38 inputs LM339 compareter inputs. Inport(0x68) reads "A"s Inport(0x69) reads "B"s.
0x6c	D0-D7	/INS	Reads U22 (D4-7) and U46 (D0-3). U46 inputs OPTO-coupler inputs. U22 inputs signals of HO5, IDX, U/D, BSY
0x70	D0-D7	/IN1	Reads H22 digital inputs
0x74	-	/LDAC	Inport(0x74) will load 4 channel buffered 12 bit DAC data into voltage output stage.
0x78	D0-D7	/HP1	Inport(0x78) reads U20 HP2020 16 bit counter high byte. inport(0x79) reads low byte.
0x7c	D0-D7	/HP2	Inport(0x7c) reads U44 HP2020 16 bit counter high byte. Inport(0x7d) reads high byte.
0x80-9f	D0-D7	LCD1	Reads H1 D0-D7
0xa0-bf	D0-D7	LCD2	Reads H1 D0-D7
0x0200	D0-D7	IO1	Reads D0-D7 for Input/Output expansion
0x0280	D0-D7	IO2	Reads D0-D7 for Input/Output expansion
0x04000	D0-D3	/TIMER	Reads U32 Real Time Clock RTC72421
0x08000	D0	/SDAI	Reads EEPROM U40 SDA data
0x0a000	D0	/PFO	Reads power failure status. If D0=1, U30 MAX691 PFI inputs < 1.3V
0x0c000	D0	/WDO	Reads Watchdog status. If D0=1, Watchdog time out

H1 IS IN MIRROR LAYOUT, VIEW FROM SOLDER SIDE

240X64 GRAPHICS LCD(TLX711/UG-24B-03GNBR)

H1

D7	1	2	D6
D5	3	4	D4
D3	5	6	D2
D1	7	8	D0
LCD1	9	10	/IOWR
A0	11	12	VLC
GND	13	14	VCC
LCD2	15	16	CAD

HDRD16
HDRD16

FOR GRAPHICS LCD: TLX711/UG-24B-03

+12V TO H1.16 MUST BE CUT FIRST !
INSTALL PAL PDP010 IN U27
LCD2=/IORD CAD=/LRST
USE PD_GLCD CABLE

SEIKO M4024

H1

D7	1	2	D6
D5	3	4	D4
D3	5	6	D2
D1	7	8	D0
LCD1	9	10	/IOWR
A0	11	12	VLC
GND	13	14	VCC
LCD2	15	16	+12V

HDRD16
HDRD16

H2

1		2	VLC

HDRD2
HDRD2

SHEET 2

SHEET 3
INPUT/KEYPADS/EEPROM

SHEET 4
AD/RS485/232

SHEET 5
POWER/HV/DAC

SHEET 6
RELAYS/OPTO

V25-ENGINE/HP

T2

DA4	1	2	DA3
DA2	3	4	DA1
AD1-	5	6	AD1+
AD2-	7	8	AD2+
AD3-	9	10	AD3+
AD4-	11	12	AD4+
AD5+	13	14	AD6+
AD7	15	16	AD8
DA	17	18	CI1

T18
T18

T1

CI2	1	2	CI3
CI4	3	4	CI5
CI6	5	6	CI7
CI8	7	8	O6
O5	9	10	O4
O3	11	12	O2
O1	13	14	485+
485-	15	16	+7V
GND	17	18	+12VI

T18
T18

J1

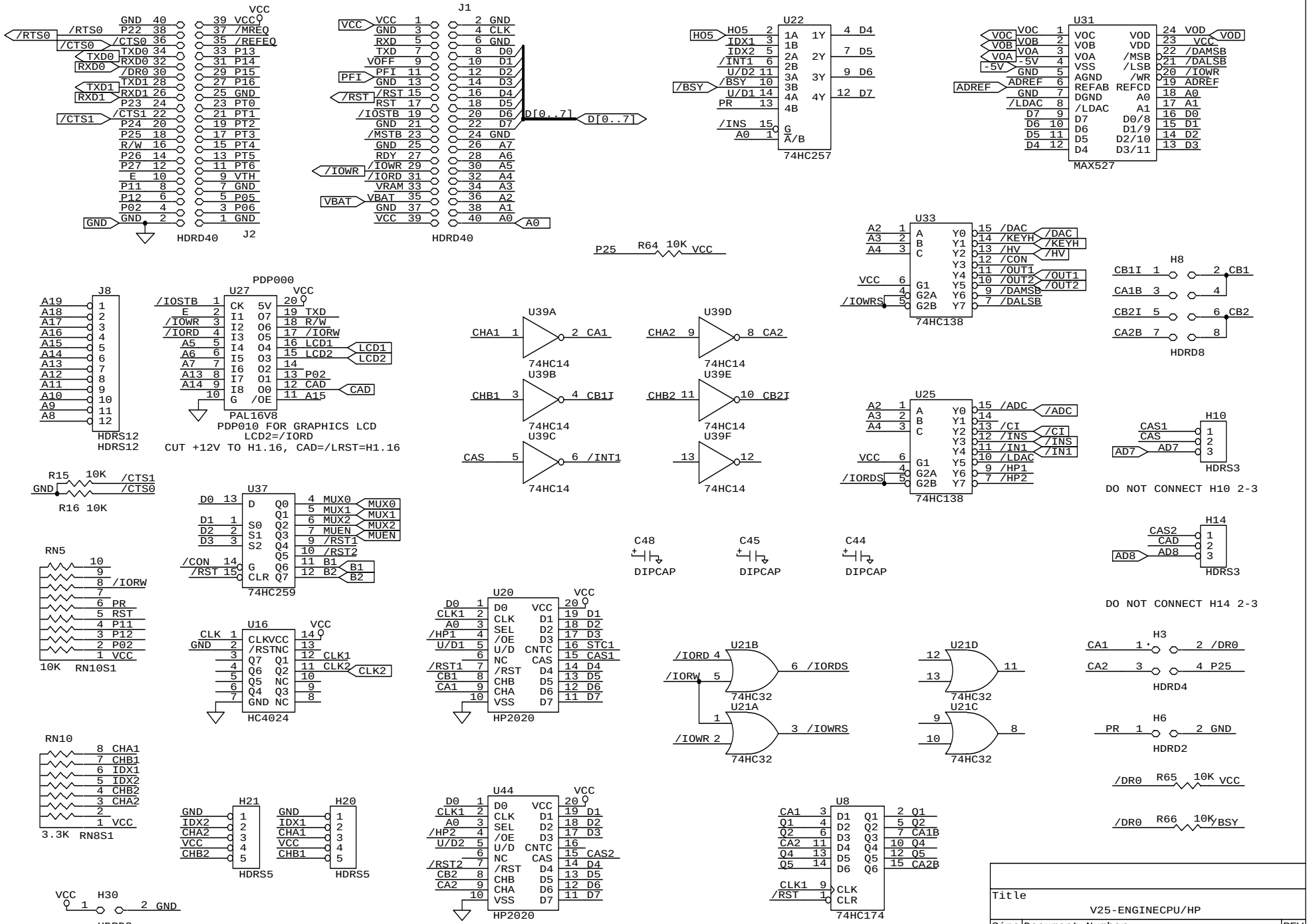
1	GND		
2			
3	+12VI		

DJ-005
DJ-005

SW
PB010
PB010

/RST
C40
0.01UF

TERN, INC.		
DAVIS CA USA		
Title	PowerDrive	
Size B	Document Number PD.SCH	REV
Date: April 4, 1995	Sheet 1 of 5	



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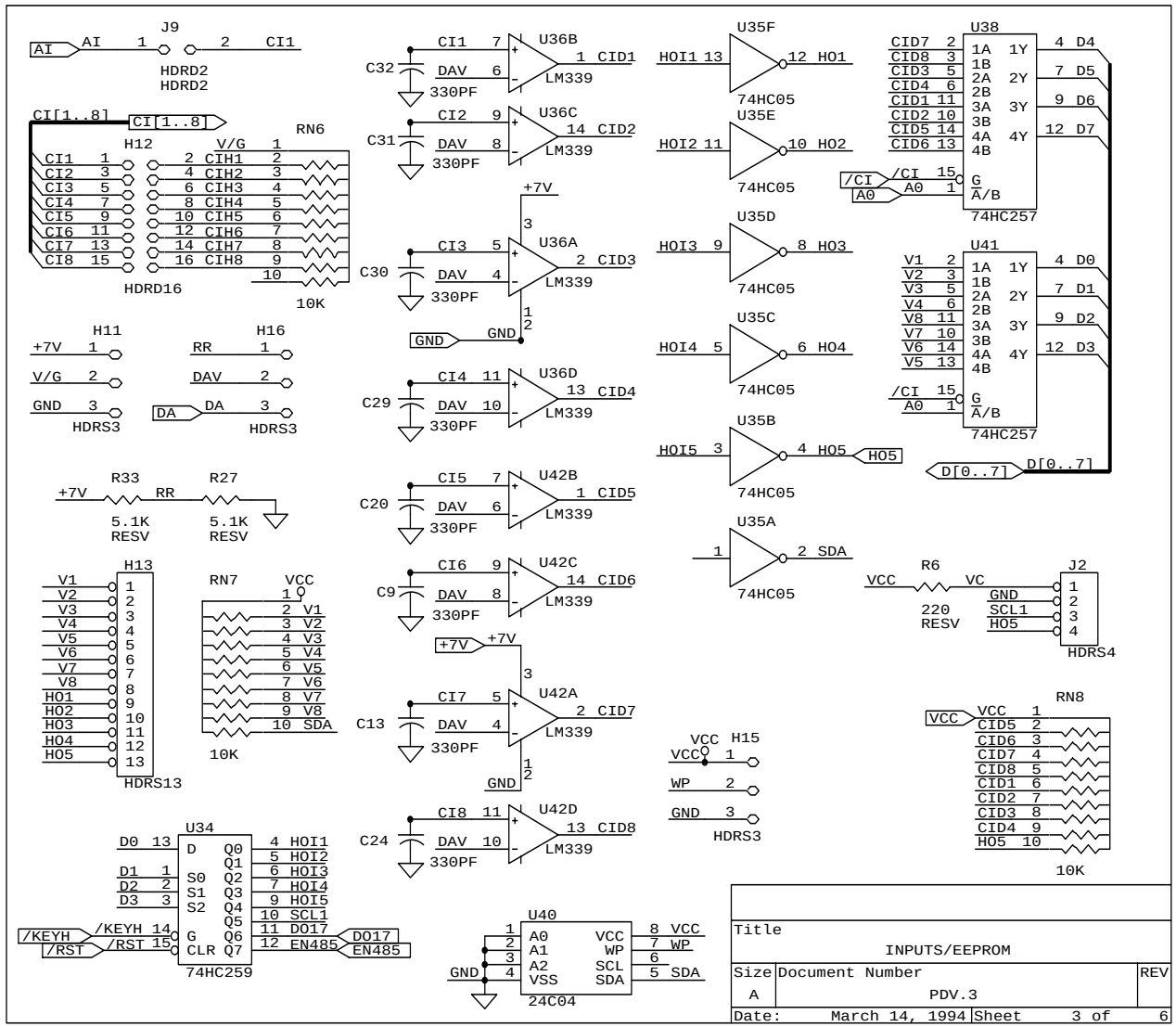
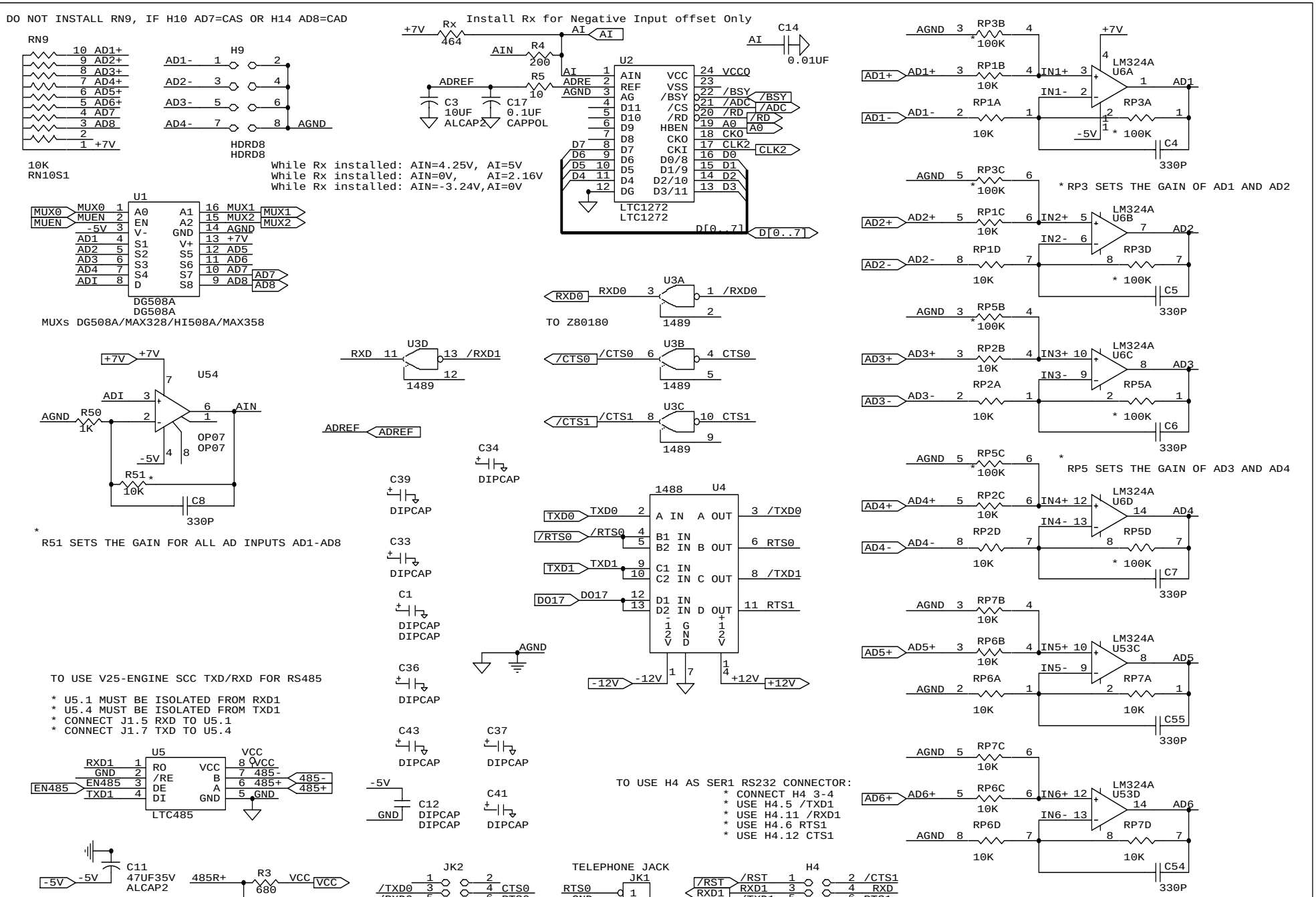
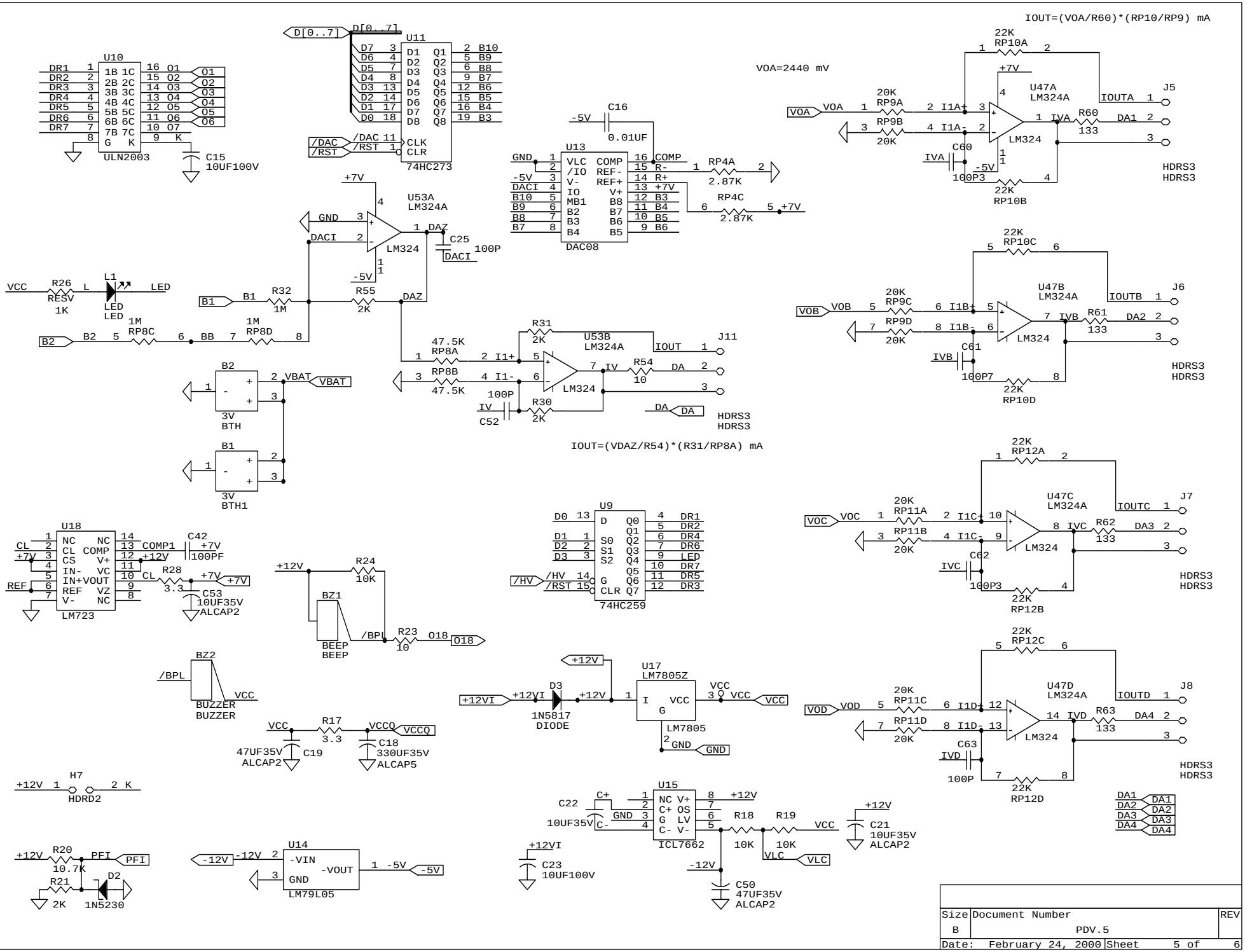
Size B	Document Number PDV.2	REV
Date: February 24, 2000	Sheet 2 of 6	


J9
AI
CI1
HDRD2
HDRD2
CI[1..8]
RN6
H12
V/G
HDRD16
10K
H11
HDRS3
H16
HDRS3
R33
R27
5.1K
RESV
5.1K
RESV
H13
HDRS13
RN7
10K
U34
74HC259
U40
24C04
U36B
U36C
U36A
U36D
LM339
330PF
C32
C31
C30
C29
U42B
U42C
U42A
U42D
C20
C9
C13
C24
U35F
U35E
U35D
U35C
U35B
U35A
74HC05
U38
U41
74HC257
D[0..7]
R6
220
RESV
J2
HDRS4
H15
HDRS3
RN8
10K
Title
INPUTS/EEPROM
Size
A
Document Number
PDV.3
REV
Date: March 14, 1994
Sheet 3 of 6


DO NOT INSTALL RN9, IF H10 AD7=CAS OR H14 AD8=CAD
RN9
10K
RN10S1
H9
HDRD8
HDRD8
Install Rx for Negative Input offset Only
While Rx installed: AIN=4.25V, AI=5V
While Rx installed: AIN=0V, AI=2.16V
While Rx installed: AIN=-3.24V,AI=0V
U2
LTC1272
LTC1272
U1
DG508A
DG508A
MUXs DG508A/MAX328/HI508A/MAX358
U3A
TO Z80180
1489
U3D
U3B
U3C
U54
OP07
OP07
R51 SETS THE GAIN FOR ALL AD INPUTS AD1-AD8
U4
1488
TO USE V25-ENGINE SCC TXD/RXD FOR RS485
* U5.1 MUST BE ISOLATED FROM RXD1
* U5.4 MUST BE ISOLATED FROM TXD1
* CONNECT J1.5 RXD TO U5.1
* CONNECT J1.7 TXD TO U5.4
U5
LTC485
TO USE H4 AS SER1 RS232 CONNECTOR:
* CONNECT H4 3-4
* USE H4.5 /TXD1
* USE H4.11 /RXD1
* USE H4.6 RTS1
* USE H4.12 CTS1
JK2
HDRD10
HDRD10
TELEPHONE JACK
JACK6
H4
HDRD12
LM324A
RP3 SETS THE GAIN OF AD1 AND AD2
RP5 SETS THE GAIN OF AD3 AND AD4
330P
DIPCAP
Title
AD/RS485/232
Size B
Document Number PDV.4
REV
Date: March 11, 1995
Sheet 4 of 6



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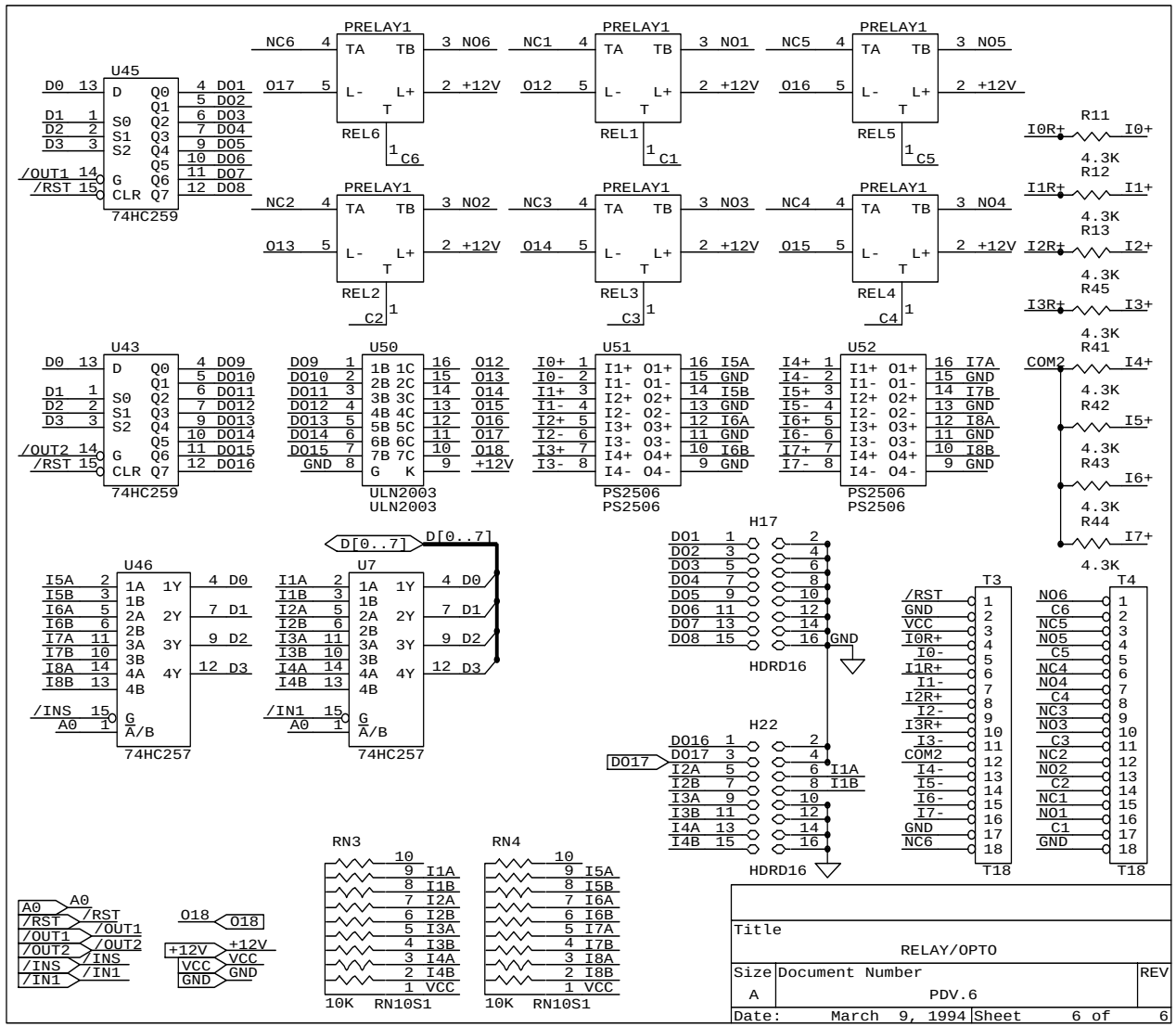
B	PDV.5	
Date: February 24, 2000	Sheet 5 of 6	


U45
74HC259
PRELAY1
REL6
REL1
REL5
REL2
REL3
REL4
C6
C1
C5
C2
C3
C4
U43
74HC259
U50
ULN2003
ULN2003
U51
PS2506
PS2506
U52
PS2506
PS2506
U46
74HC257
U7
74HC257
H17
HDRD16
H22
HDRD16
T3
T18
T4
T18
R11
R12
R13
R45
R41
R42
R43
R44
4.3K
RN3
RN4
10K RN10S1
10K RN10S1
Title
RELAY/OPTO
Size
A
Document Number
PDV.6
REV
Date: March 9, 1994
Sheet 6 of 6