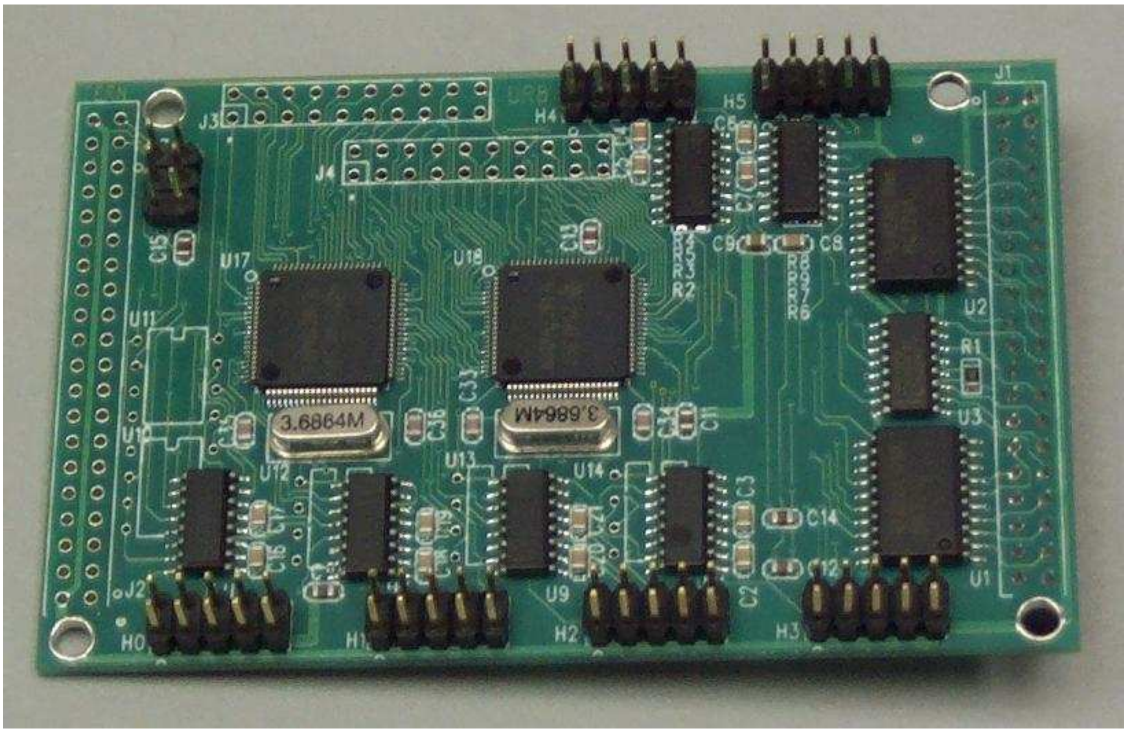
UR8 TM

Expansion Card with 8 UARTS, RS232, RS485, & RS422



Technical Manual

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Version 2.00

November 2, 2010

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

The UR8 is an expansion card designed for adding eight additional serial ports to TERN controllers. The versatility of the UR8 allows for multiple configurations, including TTL level, RS232, RS485, RS422 and can be added to any TERN controller.

The TL16C754B (two devices are installed for a total of eight UARTs) is a quad universal asynchronous receiver transmitter with 64 byte FIFOs, automatic hardware/software flow control and high-speed data rates. The deep FIFOs can release processor load and guarantee reliable performance for multi-serial port high-speed communication. It includes a transmission control register (TRC) which stores FIFO threshold levels to start/stop transmission during hardware/software control. Efficiency is also increased by using one ready register, RDY, which can return the status of all four FIFOs in one access to the device. On-chip status registers provide user with error indication, operation status, and modem interface control. An internal loop-back capability allows for on-board diagnostics. The Quad UART supports 5, 6, 7, or 8 bit communication and can generate its own baud rate based upon a divisor register and external clock input. In addition, even, odd, or no parity with 1, 1.5, or 2 stop bits are supported.

By default, a 3.6864 MHz crystal is installed as external clock input, with a 50 MHz clock input supported. The receiver can detect idle, break, or frame errors, as well as FIFO overflow and parity errors. A software interface for Modem control operation, software, and hardware flow control is included.

Of 8 total UARTs, 4 are buffered with RS232 drivers *without* handshaking signals and be optionally configured to TTL level signals, directly from the TL16C754B. The remaining 4 UARTs are buffered with RS232 drivers *with* handshaking signals. These 4 can be optional configured with RS485 drivers and one can be configured to a full-duplex 4-wire RS422 driver. All other handshaking and modem signals are TTL level and routed to two 20x2 pin headers. If the handshaking and/or modem control is not needed, these lines can be used as multi-purpose TTL level I/O.

The UR8 interfaces with other TERN controllers via the J1 8-bit address/data bus. The UR8 uses a polling method for software interface, thus not interrupt driven. Voltage-shifting circuits are on-board, allowing the UR8 to connect to a 5V or 3.3V CPU, such as the 586-Engine.

1.2 Features

- Dimensions: 3.6 x 2.3 x 0.3 inches
- Power supply input voltage: +5V **REGULATED** DC.
- Two Quad UARTs, TL16C754B, for total of 8 UARTs
- 64 byte transmit and receive FIFO for each UART
- Hardware and software flow control
- Default RS-232 drivers. TTL level, RS485, & RS422 optional.
- Installs onto J1 20x2 pin header of TERN host controller
- Handshaking/Modem Control

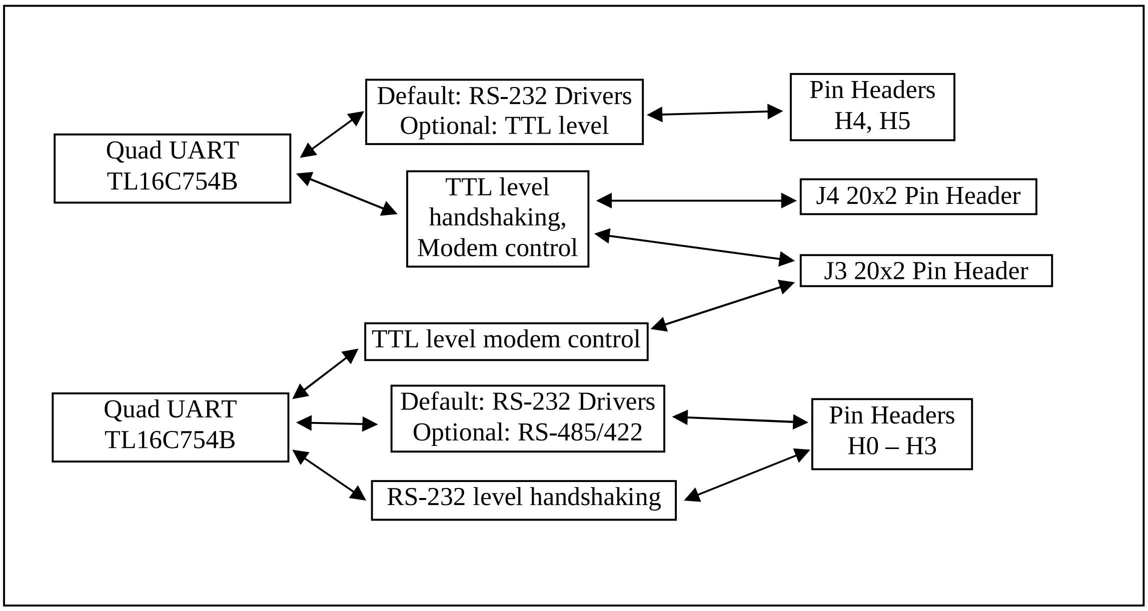
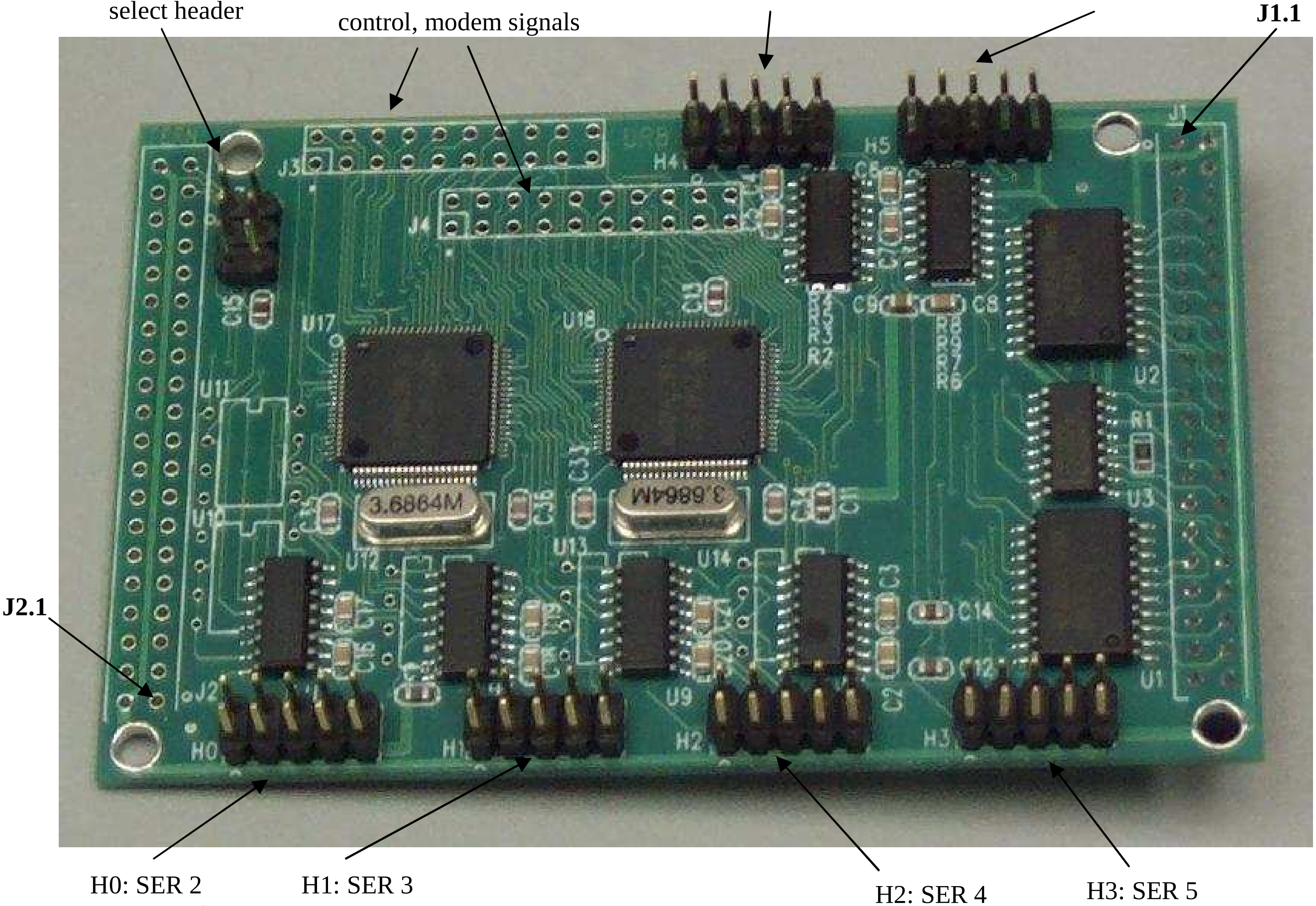


Figure 1.1 UR8 functional block diagram

1.3 Physical Description



H7: chip select header

J3 & J4: TTL level flow control, modem signals

H4: SER 6 & 7 RS232 or TTL

H5: SER 8 & 9 RS232 or TTL

J1.1

J2.1

H0: SER 2 RS232, RS485 or RS422

H1: SER 3 RS232 or RS485

H2: SER 4 RS232 or RS485

H3: SER 5 RS232 or RS485

Figure 1.2 Layout of the UR8

Chapter 2: Installation

2.1 Software Installation

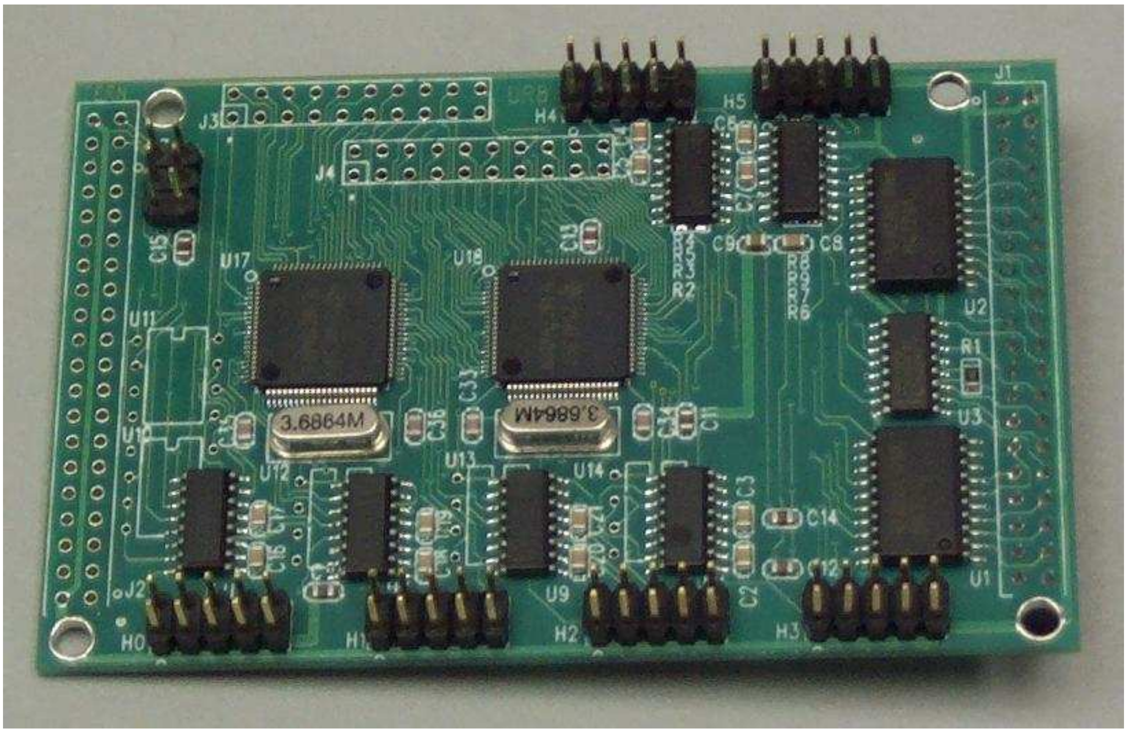
Please refer to the Technical manual for the “C/C++ Development Kit and Evaluation Kit for TERN Embedded Microcontrollers” for installing software.

The README.TXT file on the root directory of the TERN EV-P/DV-P CD contains important information about the installation and evaluation of TERN controllers.

2.2 Hardware Installation

The UART8 is an expansion board built for TERN controllers. The UART8 can be installed on the following TERN controllers: 586-Engine, A104, A104S, A-Engine, A-Engine-P, A-Engine86, A-Engine86-P, R-Engine, A-Engine86-D, BirdBox-A, i386-Engine, i386-Engine-P, i386-Engine-L, i386-Engine-M, i386-Drive, SmartLCD, and SmartLCD-Color.

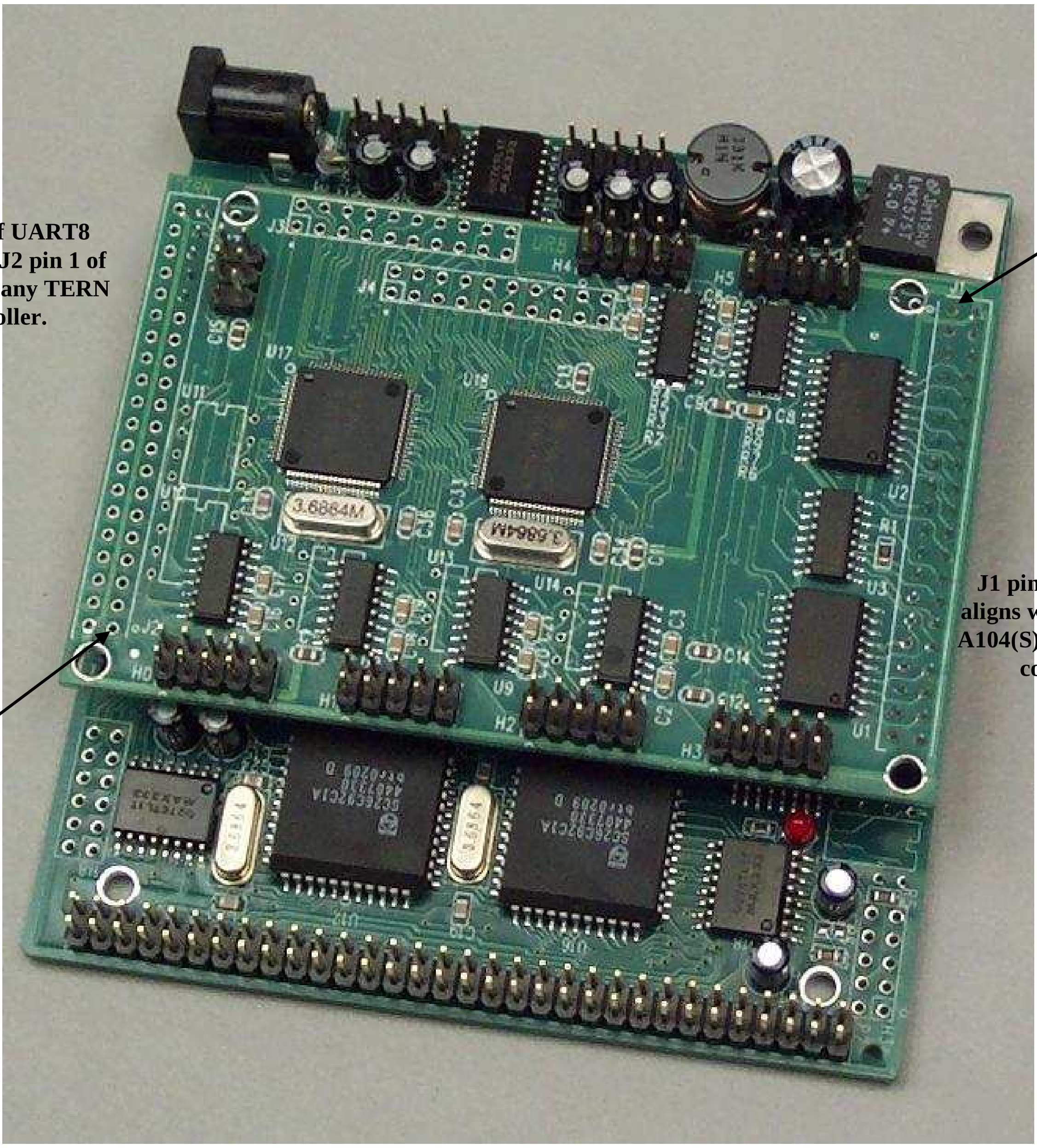
Hardware installation for the UART8 consists of installing onto its host controller. See the technical manual of the host controller for additional instructions pertaining to the host controller.



UART8 before installation onto a host controller.

2.2.1 Connecting the UART8 to the host controller

The UART8 will come installed with a 20x2 pin socket at the J1 header. In addition, it will have a 5x1 pin socket on the J2 header (pins 39,37,35,33, and 31). All that is required is to align the J1 and J2 sockets of the UART8 with the J1 and J2 pin headers of the host controller and install. It is important to align pin 1 of the corresponding headers. Each header is labeled with white letters. The pin nearest the label indicates the first pin of that header. See the following picture for an example. The UART8 is shown installed onto the A104S. Installation of the UART8 is identical for every TERN controller.



J2 pin 1 of UART8 aligns with J2 pin 1 of A104(S), or any TERN controller.

J1.1

J1 pin 1 of UART8 aligns with J1 pin 1 of A104(S), or any TERN controller.

J2.1

The UART8 installed on the A104S.

Chapter 3: Hardware / Software

The UR8 offers 8 UARTs with RS232 drivers by default. Four UARTs can be configured to RS485 and one to RS422. The following table summarizes the locations and possible configuration of each UART on the UR8.

Channel	Default Config.	Optional Config.	Handshaking	Location
2	RS232	RS485 or RS422	RS232	H0
3	RS232	RS485	RS232	H1
4	RS232	RS485	RS232	H2
5	RS232	RS485	RS232	H3
6	RS232	TTL	TTL	H4 pins 3, 5
7	RS232	TTL	TTL	H4 pins 4, 6
8	RS232	TTL	TTL	H5 pins 3, 5
9	RS232	TTL	TTL	H5 pins 4, 6

3.1 Quad UARTs

The UR8 offers two quad channel Universal Asynchronous Receiver Transmitters (UARTs). This provides a total of eight UARTs which can be added to any TERN controller. Please see complete data sheet on the TERN installation CD for full documentation, tern_docs\parts\quart_tl16c754b.pdf.

3.2 RS232 Drivers

By default, each UART on the UR8 comes buffered with RS232 drivers. Four UARTs offer RS232 level handshaking, while four offer only TTL level handshaking. For complete details, please see the full data sheet on the TERN installation CD, tern_docs\parts\max232.pdf.

3.3 RS485 Drivers

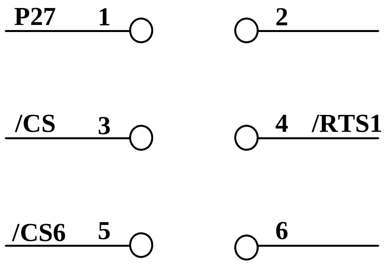
The UR8 allows for optional configuration on four UARTs to RS485 drivers for networking. In additional one channel can be configured to RS422 to provide a 4-wire full-duplex port. The complete date sheet is on the TERN installation CD, tern_docs\parts\sn75tlc184.pdf.

3.4 Software

Sample code is provided for the UR8. If using a TERN controller with a 186 CPU, UR8 sample code can be found in the tern\186\samples\ur8 directory. If your TERN controller uses the i386EX, find sample code in the tern\386\samples\ur8 directory. If using the 586-Engine, see tern\586\samples\ur8. Sample projects have been created also. The project ur8_echo.ide can be found in the tern\186, tern\386 and tern\586 directories.

3.5 Chip Selects

The UR8 was designed for any TERN controller. Different TERN controllers use different peripheral chip select lines and are found in different locations at the pin header. The UR8 is thus equipped with a pin header to allow the user to choose which chip select from the host controller will be used, depending on the host controller and configuration. See schematic at the end of this manual of additional details.



Above shows the H7 pin header on the UR8. Pin 3 = /CS is routed to an 8 channel decoder on the UR8 to generate 8 unique chips selects, one for each UART. Pins 1, 4 and 5 represent three possible signals from the host controller, with the function depending on which host controller is used. The user must tie one of these three pins via jumper to the UR8 chips select (/CS). Three sections below will summarize the possible configurations based on CPU. Regardless of CPU, the user should confirm the correct address selection in the UR8 header file (ur8.h) to match the hardware selection.

186 Based Boards:

There are two chips selects on the 186 based boards which are routed to the H7 header of the UR8, giving 2 different chip select configurations. Pin 5 (/CS6 on the UR8) comes from J1.19 (P16) on the 186 based boards (AE, AE86, BBA, A104, etc.). Pin 4 (/RTS1 on the UR8) comes from J2.33 (/RTS1) on the 186 based boards. For the 186 boards, the default configuration will use /RTS1, and thus H7.3 = H7.4, as H7.5 (/CS6) = J1.19 (P16) is already reserved for other TERN expansion boards, such as the P100 and the P50. If necessary, the user may use /CS6 as the chip select, provided the P50 or P100 is not used and the proper jumper is installed (H7.3 = H7.5).

The BBA is a special case. On the BBA, P16 is used as the chip select for the U16 PPI chip, and /RTS1 = /PCS3 is used for an HC259. To interface the UR8, one device (PPI or HC259) on the BBA must be sacrificed. The default configuration, H7.3=H7.4, does not require hardware modification on the BBA, yet the HC259 cannot be used (its output will be garbage). If the user requires the HC259 but not the U16 PPI for application, the H7.3 = H7.5 (/CS6) can be used only if the U16 PPI on the BBA is disabled. Setting H7.3 = H7.5 without disabling the U16 PPI will cause two devices to simultaneously occupy the bus and the controller will crash.

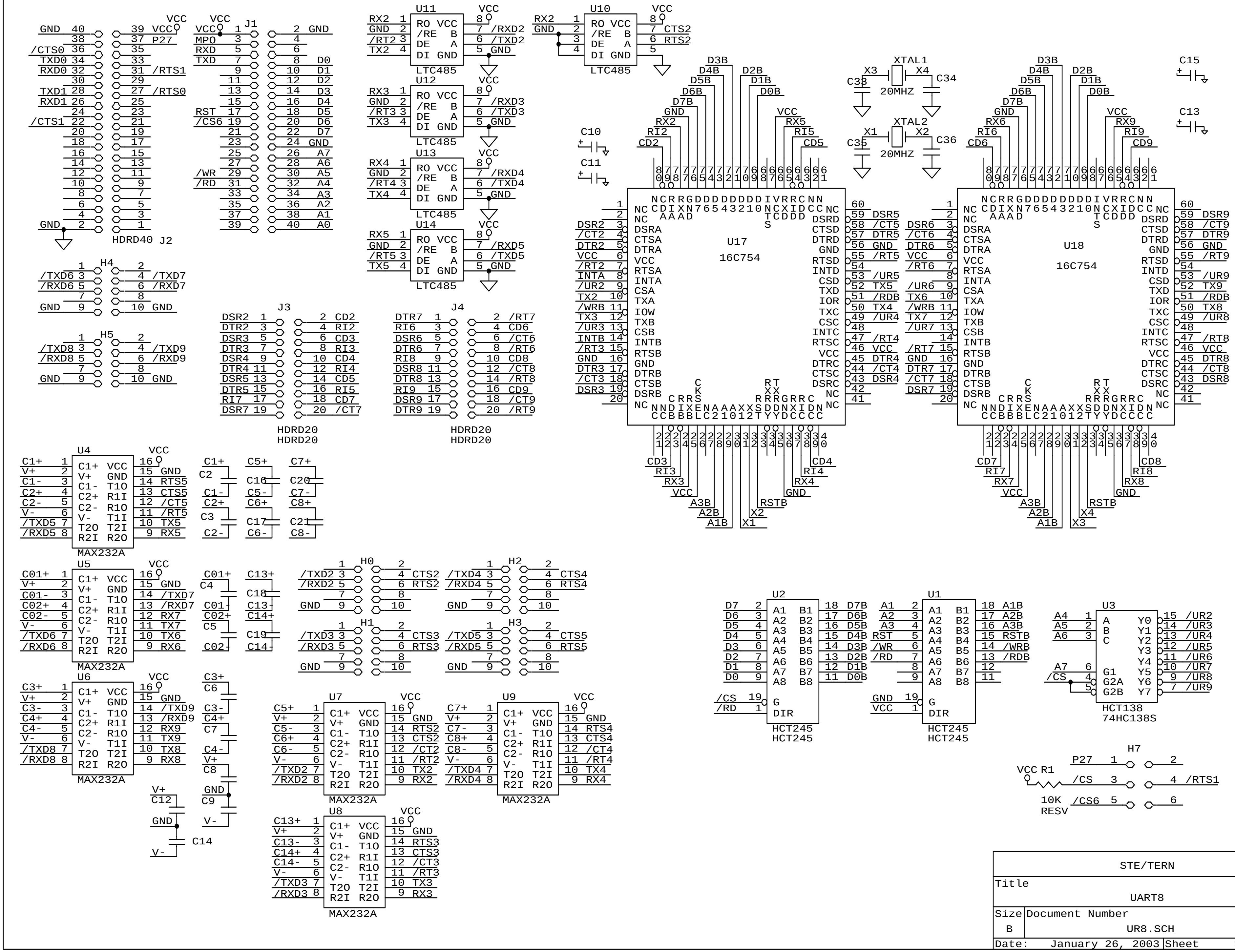
The SmartLCD-Color (SLC) is another controller based on the 186 CPU which requires special modification. In this case, the hardware counter on the SLC (location U37) must be disabled. This can be done by lifting U37.24 and tying to VCC. On the UR8, a larger expansion socket must be used on the J2 pin header (it must include J2.22). In addition, a wire jumper must be installed from J2.22 to H7.3. Finally, two software modifications must be completed. First, use the statement “define UR8_BASE 0x200” in the header file tern\186\include\ur8.h. Secondly, the statement “pio_init(18,0)” must be added to all UR8 sample code before access to the UR8.

386 Based Boards:

The 386 based boards have two chip selects routed to the UR8. J1.19 = /CS6 is already reserved for the P100, while J2.37 = P21 = /CS1 is reserved for the P50. If either the P100 or the P50 is being used in conjunction with the UR8, the un-reserved chip select must be used to drive the UR8. It is also necessary to select the corresponding I/O address for the chip select on the tern\386\include\ur8.h header file.

586-Engine:

The 586-Engine has two chip select signals routed to the UR8 H7 header. J1.19 = /CS6 is reserved when using the 586-Engine + P100 and J2.37 = P27 is reserved when using the 586-Engine + P50. If neither the P50 nor the P100 are being used, either chip select can be used, with the matching jumper at H7 and the matching I/O address in the UR8 header file (tern\586\include\ur8.h). If the 586-Engine is driving the P100 or the P50 and the UR8, the UR8 must use the unused chip select. Whichever chip select is used, the corresponding jumper must be set on the UR8 and the correct I/O address set in the header file (tern\586\include ur8.h).



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Size B	Document Number UR8.SCH	REV
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