

*V25-Engine*TM

C/C++ Programmable 16-bit Microprocessor Module
Based on the NEC V25

*C-Engine*TM

C/C++ Programmable, 16-bit Microprocessor Module
with
11 channels of 12-bit ADC



Technical Manual



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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

The *V25-Engine (VE)/C-Engine (CE)* from TERN are low cost, high performance, C/C++ programmable, 16-bit microprocessor core modules. They are designed for embedded applications that require compactness, low power consumption, and high reliability. The *V25-Engine/C-Engine* can be integrated into an OEM product as a processor core component. They can also be used to build a smart sensor, or used as a node in a distributed microprocessor system.

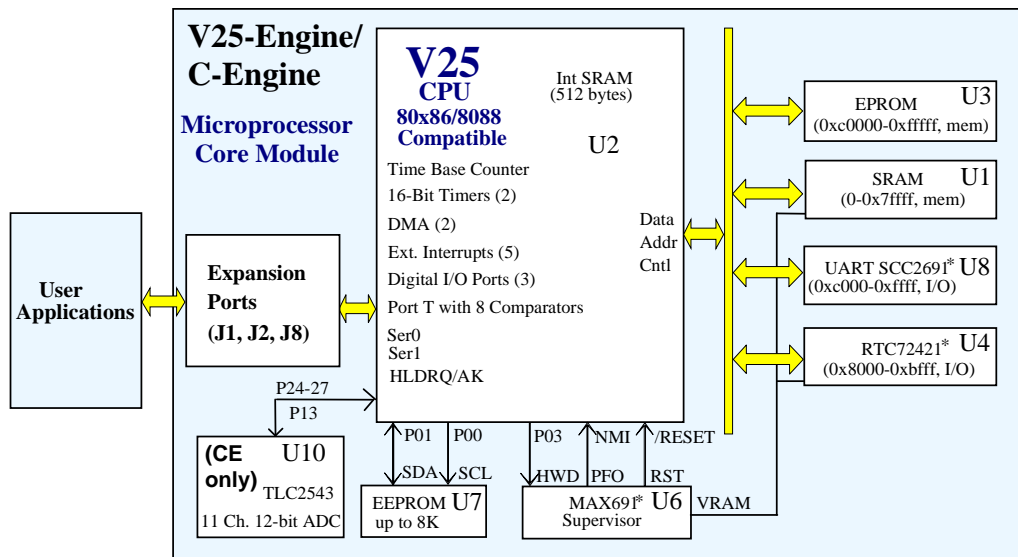


Figure 1.1 Functional block diagram of the V25-Engine/C-Engine

Measuring 3.6 x 2.3 x 0.3 inches, the *V25-Engine/C-Engine* offer a complete C/C++ programmable computer system with a 16-bit high performance CPU (NEC V25) and operate at 8 MHz with zero-wait-states. Optional features include up to 512K EPROM/Flash and up to 512K battery-backed SRAM. A 512-byte serial EEPROM is included on-board. An optional real-time clock provides information on the year, month, date, hour, minute, second, and 1/64 second, and an interrupt signal.

Two DMA-driven serial ports from the NEC V25 support high-speed, reliable serial communication at a rate of up to 115,200 baud. An optional UART SCC2691 may be added in order to have a third UART on-board. All three serial ports support 8-bit and 9-bit communication.

The optional *12-bit ADC* (available on the *C-Engine*) has 11 channels of analog inputs with sample-and-hold and a high-impedance reference input (2.5-5V) that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise.

The optional *VE232* provides regulated 5V power and RS232/RS485 drivers for the *V25-Engine/C-Engine*. The *VE/CE* can also be installed on TERN controllers, such as the *P300*, *PowerDrive*, *PC-Co*, *SensorWatch*, or *MotionC* (see Figure 1.2) to provide regulated 5V power and RS232/RS485 drivers. TERN also offers custom hardware and software design, based on the *V25-Engine* or other TERN controllers.

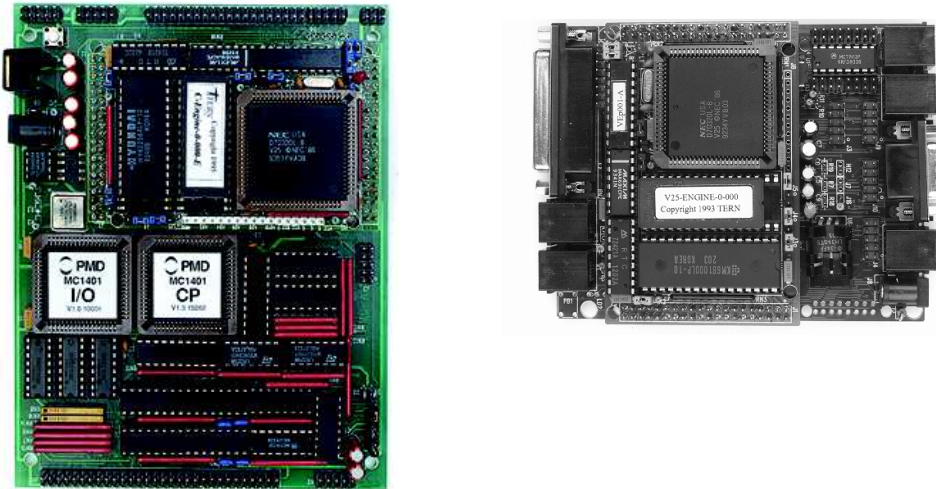


Figure 1.2 The V25-Engine installed on the MotionC (left) and on the BirdBox (right)

1.2 Features

Standard Features

- Dimensions: 3.58 x 2.30 x 0.50 inches
- Power consumption: 75 mA full speed, 30 mA standby (with standard parts)
- Low power version: 55 mA full speed, 3 mA standby (with low power parts)
- Power Input: +5V regulated DC without VE232
+9V to +12V unregulated DC with VE232
- 16-bit CPU (NEC V25), 8 MHz, Intel 80x86 compatible, C/C++ programmable
- ROM and SRAM up to 1MB, 512-byte EEPROM (or up to 2KB) and 256 bytes built-in-CPU SRAM
- Five external interrupts, 24 bi-directional digital I/O lines, 8 comparators (some are used by system)
- Two 16-bit timers, one 16-bit time base counter
- Two 16-bit counters or DMA. The counter can count external signal rising edges up to 500 KHz
- Two high speed serial ports from the V25 CPU
- Supervisor chip (691) for power failure, reset and watchdog

Optional Features:

- 32KB, 128KB, or 512KB SRAM
- 11 channels of 12-bit ADC, sample rate up to 10 KHz
- SCC2691 UART (on-board) supports 8-bit or 9-bit networking
- Real-time clock RTC72423, lithium coin battery
- VE232 add-on board for regulated 5V power & RS232/RS485 drivers



Figure 1.3 VE232 interface board

1.3 Physical Description

The physical layout of the V25-Engine/C-Engine is shown in Figure 1.4.

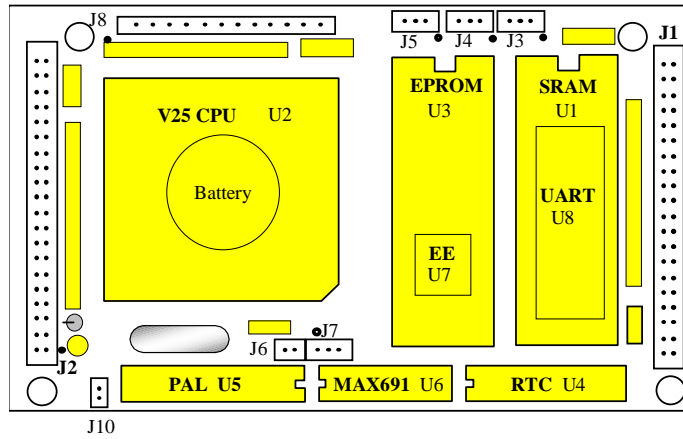


Figure 1.4 Physical layout of the V25-Engine

The physical layout of the C-Engine™ is shown in Fig. 1.5. The components with dashed line shown in Fig. 1.2 are located underneath other chips. The small circles denote the PIN 1 positions.

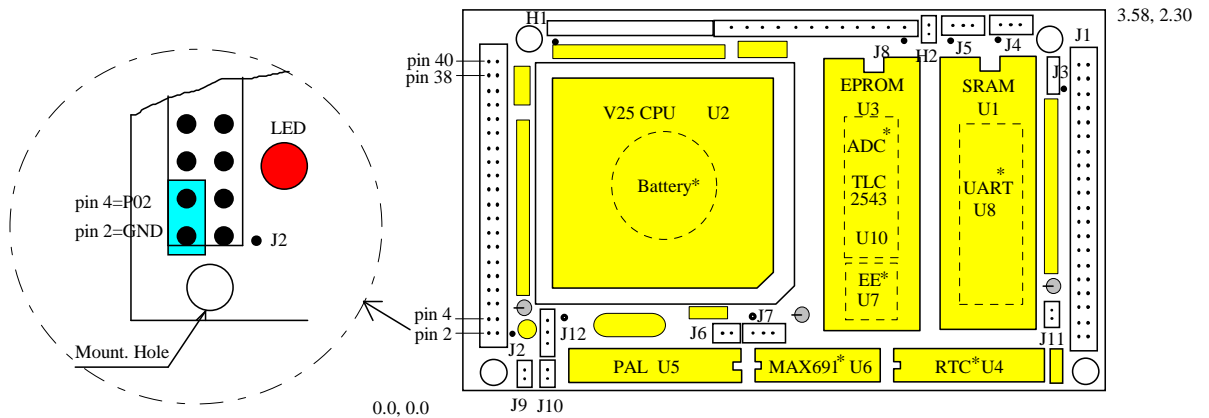
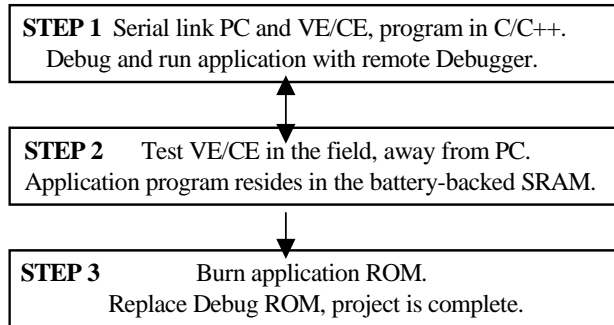


Figure 1.5 Physical layout of C-Engine™. The components with "*" are optional.

1.4 V25-Engine/C-Engine Programming Overview

Development of application software for the V25-Engine/C-Engine consists of three easy steps:



You can program the V25-Engine/C-Engine from your PC via serial link with an RS232 interface. Your C/C++ program can be remotely debugged over the serial link at a rate of 115,000 baud. The C/C++ Evaluation Kit (EV) or Development Kit (DV) from TERN provides a Borland C/C++ compiler, TASM, LOC31, Turbo Remote Debugger, I/O driver libraries, sample programs, and batch files. These kits also include a DEBUG ROM (*TDREM_V25*) to communicate with Turbo Debugger, a DB9-IDE10 (PC-V25) serial cable to connect the controller to the PC, and a 9-volt wall transformer. See your *Evaluation/Development Kit Technical Manual* for more information on these kits.

After you debug your program, you can test run the V25-Engine/C-Engine in the field, away from the PC, by changing a single jumper, with the application program residing in the battery-backed SRAM. When the field test is complete, application ROMs can be produced to replace the DEBUG ROM. The .HEX or .BIN file can be easily generated with the makefile provided. You may also use the DV Kit or ACTF Kit to download your application code to on-board Flash.

The three steps in the development of a C/C++ application program are explained in detail below:

STEP 1: Debugging

- Write your C/C++ application program in C/C++.
- Connect your controller to your PC via the PC-V25 serial link cable.
- Use the batch file **m.bat** to compile, link, and locate, or use **t.bat** to compile, link locate, download, and debug your C/C++ application program.

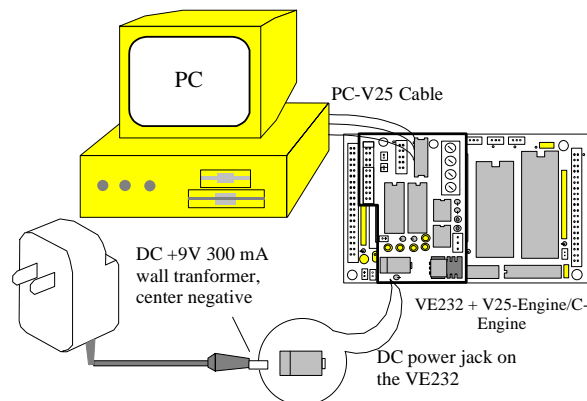


Figure 1.5 Step 1 connections for the V25-Engine/C-Engine

STEP 2: Standalone Field Test.

- Set the jumper on J2 pins 2 and 4 on the V25-Engine/C-Engine (Figure 1.6).
- At power-on or reset, if J2 pin 4 (P02) is low, the CPU will run the code that resides in the battery-backed SRAM.
- If a jumper is on J2 pins 2-4 at power-on or reset, the VE/CE will operate in Step Two mode. If the jumper is off J2 pins 2-4 at power-on or reset, the VE/CE will operate in Step One mode. The status of J2 pin 4 (signal P02 of the NEC V25) is only checked at power-on or at reset.

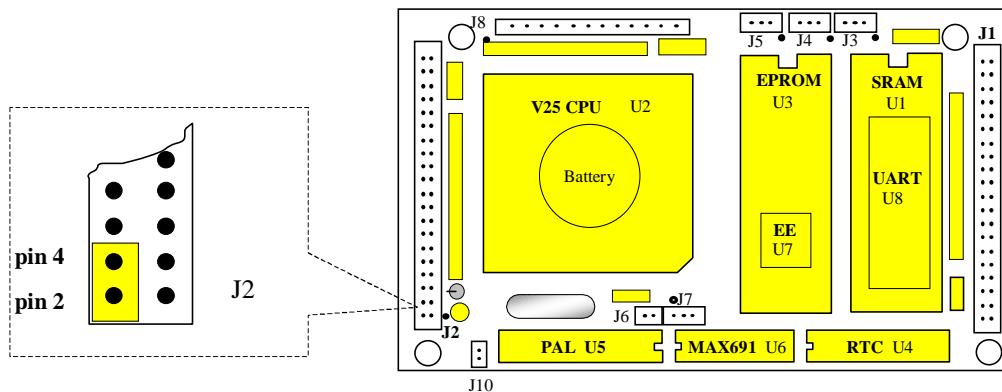


Figure 1.6 Location of Step 2 jumper on the V25-Engine/C-Engine

STEP 3: Generate the application .BIN or .HEX file, make production ROMs or download your program to FLASH via ACTF.

- If you are happy with your Step Two test, you can go back to your PC to generate your application ROM to replace the DEBUG ROM (*TDREM_V25*). You need to change **DEBUG=1** to **DEBUG=0** in the makefile.

You need to have the DV Kit to complete Step Three.

Please refer to the Tutorial of the Technical Manual of the EV/DV Kit for further details on programming the V25-Engine/C-Engine.

1.5 VE232

The VE232 is an interface board for the V25-Engine/C-Engine that provides regulated +5V DC power and RS232/485 drivers. It converts TTL signals to and from RS232 signals. You do not need the VE232 if you are using the V25-Engine/C-Engine installed on another TERN controller such as the P300, PC-Co, MotionC, PowerDrive, or SensorWatch.

The VE232, shown in Figure 1.7, measures 2.3 x 1.57 inches. A wall transformer (9V, 300 mA) with a center negative DC plug ($\varnothing=2.0$ mm) should be used to power the VE/CE via the VE232. The VE232 connects to VE/CE via H1 (2x10 header). SER0 (J2) and SER1 (J3) on the VE232 are 2x5-pin headers for serial ports SER0 and SER1. SER0 is the default programming port.

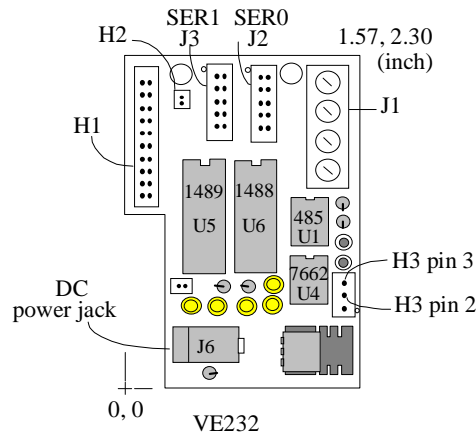


Figure 1.7 The VE232, an interface card for the V25-Engine/C-Engine

For further information on the VE232, please refer to Appendix B and to the VE232 schematic at the end of this manual.

1.6 Minimum Requirements for V25-Engine/C-Engine System Development

1.6.1 Minimum Hardware Requirements

- PC or PC-compatible computer with serial COMx port that supports 115,200 baud
 - V25-Engine/C-Engine controller with DEBUG ROM *TDREM_V25*
 - VE232 interface board *
 - DB9-IDE10 (PC-V25) serial cable (RS232; DB9 connector for PC COM port and IDC 2x5 connector for controller)
 - center negative wall transformer (+9V 500 mA)
- * NOTE: the VE232 is not needed if you are using the VE/CE installed on another controller

1.6.2 Minimum Software Requirements

- TERN EV/DV Kit installation diskettes
- PC software environment: DOS, Windows 3.1, Windows95, or Windows98

The C/C++ Evaluation Kit (EV) and C/C++ Development Kit (DV) are available from TERN. The EV Kit is a limited-functionality version of the DV Kit. With the EV Kit, you can program and debug the V25-Engine/C-Engine in Step One and Step Two, but you cannot run Step Three. In order to generate an application ROM/Flash file, make production version ROMs, and complete the project, you will need the Development Kit (DV).

Chapter 2: Installation

2.1 Software Installation

Please refer to the Technical manual for the “C/C++ Development Kit and Evaluation Kit for TERN Embedded Microcontrollers” for information on installing software.

The README.TXT file on the TERN EV/DV disk contains important information about the installation and evaluation of TERN controllers.

2.2 Hardware Installation

Overview

- Install VE232 (if applicable):
H1 connector of VE232 installs on J2 of the V25-Engine
- Connect PC-V25 cable:
For debugging (Step One), place connector on SER0 with red edge of cable at pin 1
- Connect wall transformer:
Connect 9V wall transformer to power and plug into power jack

Hardware installation for the V25-Engine/C-Engine consists primarily of connecting the microcontroller to your PC. The VE232 must be used to supply regulated power and RS232 drivers to the V25-Engine/C-Engine. If the V25-Engine/C-Engine is installed on another controller, please refer to the technical manual for that controller’s installation information.

2.2.1 Connecting the VE232 to the Engine

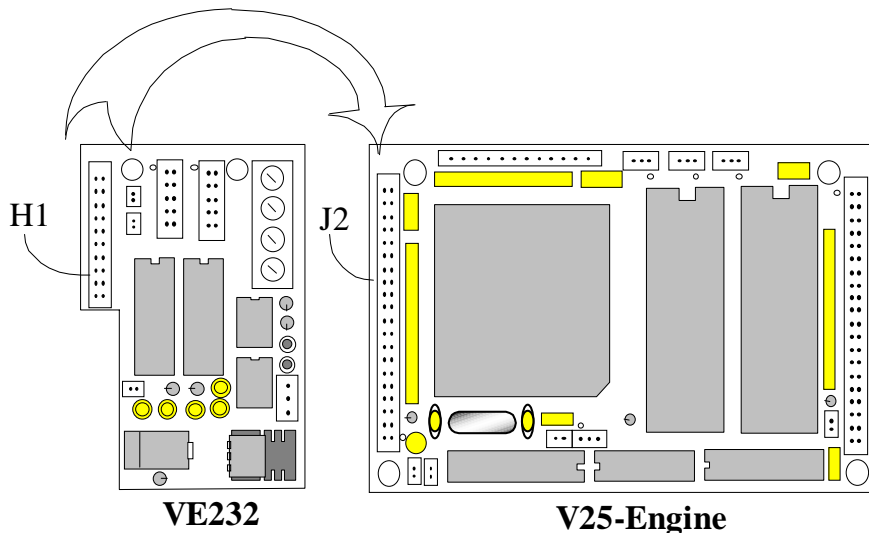


Figure 2.1 Before installing the VE232 on the Engine

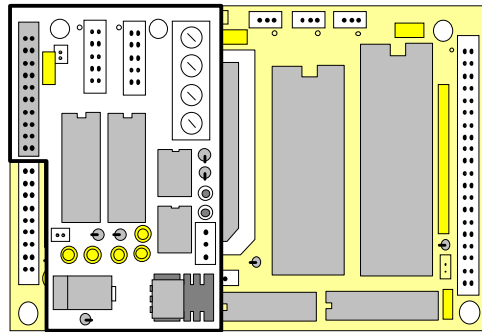


Figure 2.2 After installing the VE232 on the V25-Engine

Install the VE232 interface with the H1 (10x2) socket connector on the upper half of the J2 (dual row header) of the V25-Engine. Figure 2.1 and Figure 2.2 show the VE232 and the V25-Engine before and after installation.

2.2.2 Connecting the V25-Engine or C-Engine to the PC

The following diagram (Figure 2.3) illustrates the connection between the V25-Engine/C-Engine, VE232, and the PC. The Engine is linked to the PC via a serial cable (PC-V25).

The TDREM_V25 DEBUG ROM communicates through SER0 by default. Install the 5x2 IDC connector on the SER0 header of the VE232. **IMPORTANT:** Note that the red side of the cable must point to pin 1 of the VE232 H1 header. The DB9 connector should be connected to one of your PC's COM Ports (COM1 or COM2).

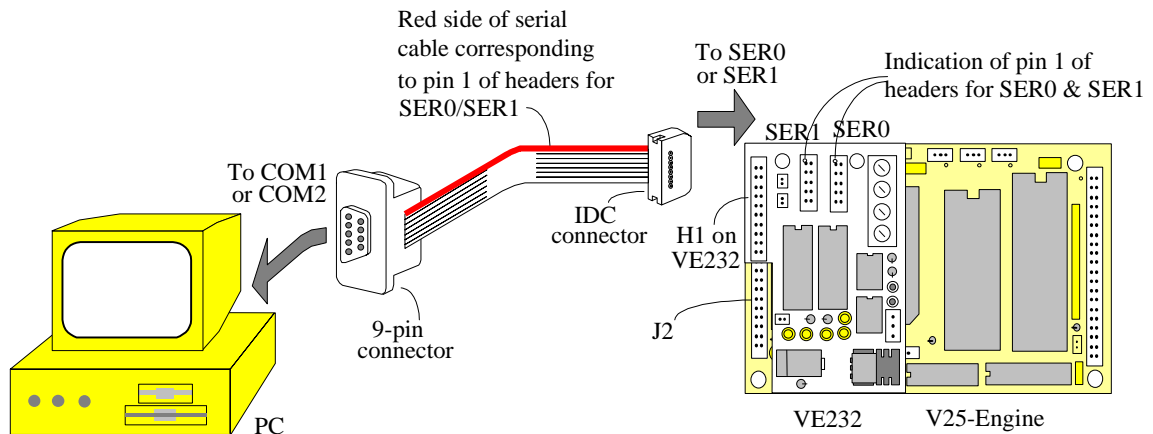


Figure 2.3 Connecting the Engine and VE232 to the PC

2.2.3 Powering-on the V25-Engine/ C-Engine

Connect a wall transformer +9V DC output to the VE232 DC power jack.

The on-board LED should blink twice and remain on after the V25-Engine/C-Engine is powered-on or reset (Figure 2.4).

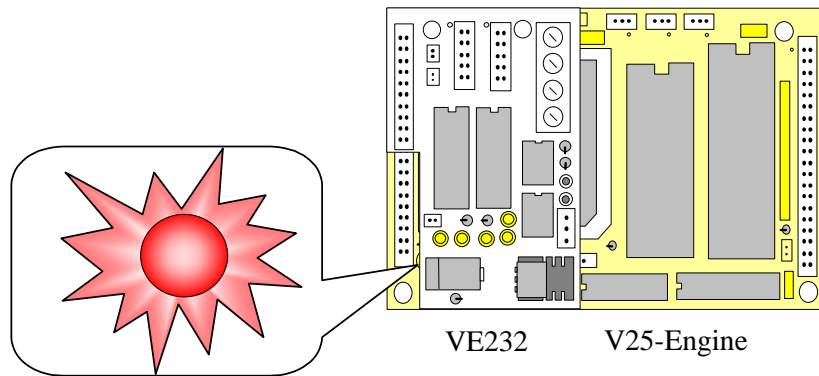


Figure 2.4 The LED blinks twice after the V25-Engine/C-Engine is powered-on or reset

Chapter 3: Hardware

3.1 NEC V25 - Introduction

The NEC V25 is based on industry-standard x86 architecture. The NEC V25 controllers are a higher-performance, more integrated versions of the 80C188 microprocessors. In addition, the NEC V25 has new peripherals including 256 bytes built-in RAM, high speed serial ports, parallel I/O ports, comparator ports, timers, and DMA. The on-chip system interface logic can minimize total system cost.

3.2 NEC V25 – Features

3.2.1 Clock

Due to its integrated clock generation circuitry, the NEC V25 microcontroller allows the use of a selectable system clock frequency of $f_x/2$, $f_x/4$ and $f_x/8$. The design achieves a maximum 8 MHz CPU operation, while using a 16 MHz crystal.

The system CLKOUT signal is routed to J1 pin 4, defaulted to 8 MHz.

3.2.2 External Interrupts

There are five external interrupts: /INTP0-/INTP2, NMI, and INT.

/INTP0 = P11, J2 pin 8, is used by the SCC2691 UART, if it is installed.

/INTP1 = P12, J2 pin 6

/INTP2 = P13, J2 pin 33

/NMI = P10, J2 pin 7

/INT = P14, J2 pin 31

INTP0 to INTP2 and NMI are edge-detected interrupts, and INT is level-detected. The valid edge for each edge-sensitive interrupt can be specified in a special function register. Valid edges for these interrupts are found in the *INTM* register (Interrupt Mode Register. Page 98 in the NEC V25 User's Manual).

NMI and INT are special external interrupts. NMI cannot be disabled and therefore is the highest-priority interrupt that can be detected. INT is an active, high-level sensitive interrupt that is not subject to multiple servicing control by the interrupt controller. INT is always acknowledged if interrupts are enabled.

The V25-Engine uses vector interrupt functions to respond to external interrupts. Refer to the NEC V25 User's Manual for information about interrupt vectors.

3.2.3 Asynchronous Serial Ports

The NEC V25 CPU has two asynchronous serial channels: SER0 and SER1. Both asynchronous serial ports support the following:

- Full-duplex operation
- 7-bit and 8-bit data transfers
- Odd, even, and no parity
- One or two stop bits
- Error detection
- Hardware flow control
- Transmit and receive interrupts for each port
- Independent baud rate generators

The software drivers for each serial port implement a ring-buffered macro service receiving and ring-buffered interrupt transmitting arrangement. See the sample files `s1_echo.c` and `s0_echo.c`.

An optional external SCC2691 UART is located in U8, underneath the SRAM (U1). For more information about the external UART SCC2691, please refer to section 3.4.3 and Appendix C.

3.2.4 Timer Control Unit

The NEC V25 CPU has two 16-bit programmable timers: Timer 0 and Timer 1. Both programmable 16-bit timers are comprised of a 16-bit modulo register, a 16-bit timer register, and an 8-bit control register.

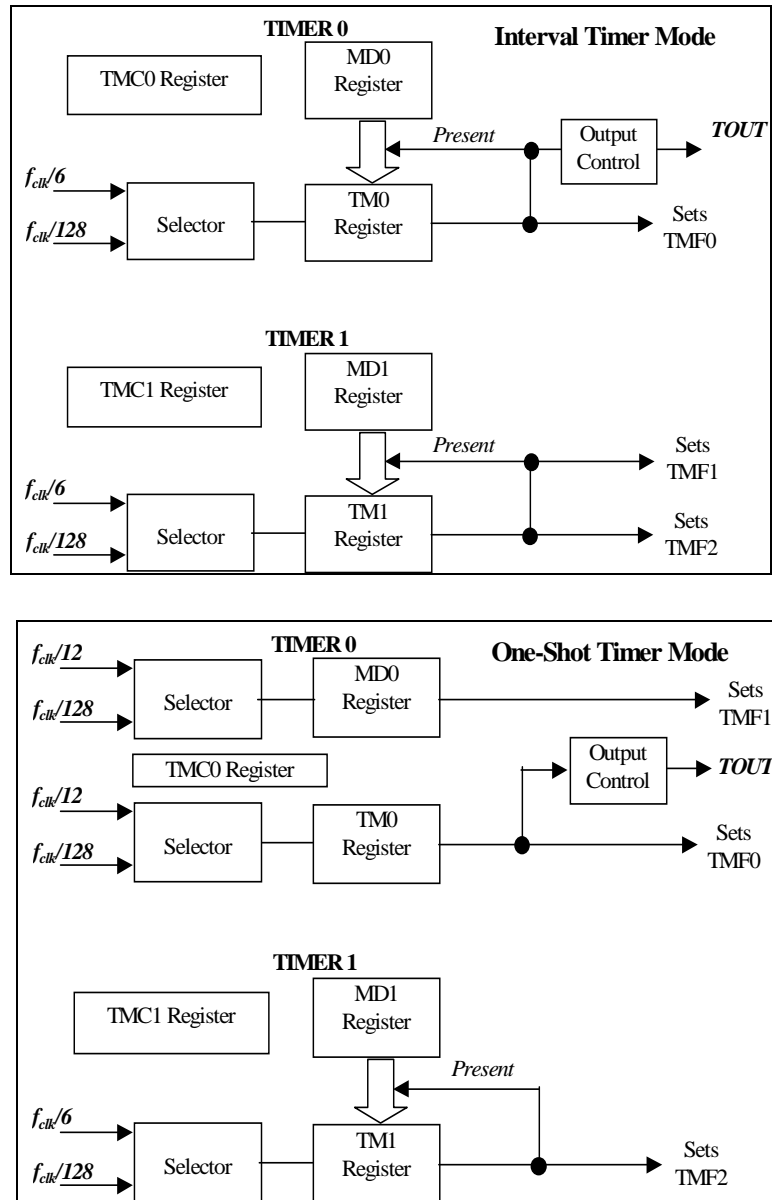


Table 3.1 Interval Timer Mode and One-Shot Timer Mode Configuration

Timer0 can be programmed as an interval timer or as a one-shot timer. In interval timer mode, the MD0 register value is set to the TM0 register, and then the TM0 countdown begins (Table 3.1). When TM0

underflows, the TMF0 output is set to 01 and the MD0 register is again set to TM0. The countdown clock, f_{clk} , is divided by 6 or 128, as defined in the TMC0 register. The square wave generated by Timer0 can be output to **TOUT** (J2 pin 29 = P15).

As a one-shot timer, Timer 0 is configured as two independent timers that count down from the value set in MD0 and TM0 (Table 3.1). The countdown frequency is divided by 12 or 128. If the counter is stopped by either reaching 0 in the count or by setting the TS0 bit to 0 (STOP = 0), a single pulse outputs at **TOUT**.

Timer1 can only act as an interval timer and has no external output.

3.2.5 Standby Modes

The V25-Engine is an ideal core module for applications that require low power consumption. The V25 CPU has two standby modes, HALT and STOP mode, which reduce power consumption and heat dissipation, thereby extending battery life in portable systems.

In HALT or STOP mode, operation of the CPU clock is stopped and program execution is halted. All registers and RAM content are preserved. HALT mode can drop the power consumption to 50 mA. When an interrupt occurs, it automatically returns to normal operation.

The difference between HALT mode and STOP mode is that HALT mode allows peripheral hardware (such as serial ports, DMA controller, etc.) to function. STOP mode disables all devices. The following table shows which devices are active and which are inactive during HALT and STOP modes.

| Item | HALT Mode | STOP Mode |
|------------------------------|---------------|---------------|
| Oscillator | Operates | Stops |
| Internal System Clock | Stops | Stops |
| 16-bit timer | Operates | Stops |
| Time Base counter | Operates | Stops |
| HOLD circuit | Operates | Stops |
| Serial interface | Operates | Stops |
| Interrupt request controller | Operates | Stops |
| DMA controller | Operates | Stops |
| I/O lines | Data Retained | Data Retained |

Table 3.2 Hardware Status During Standby Mode

To release stop mode, /NMI or /RESET must be triggered. A non-maskable interrupt request, DMA request, macro service request, or a reset will release HALT mode. Since the serial ports are functional during HALT mode, it is possible to send a break command to the serial port to resume operations.

3.3 NEC V25 I/O Ports

3.3.1 Port 0, 1, and 2

The NEC V25 has three 8-bit user-programmable I/O ports available. The 24 bi-directional I/O ports (0-2) are multiplexed with different functions. Individual I/O lines can be specified as an input, output, or control line. Each port is controlled by a Port Mode Control Register (PMC), a Port Mode Register (PM), and a Port Data Register (P). You can write or read these registers via the following functions:

or `pokeb(0xffff0, 0x??, 0x!!)`
`peekb(0xffff0, 0x??)`

where ?? is the register offset address and !! is the control/data byte.

The following is a list of the register addresses.

| Register Symbol | Register Offset Address | R/W | Access Units (bits) |
|-----------------|-------------------------|-----|---------------------|
| P0 | 0x00 | R/W | 8/1 |
| PM0 | 0x01 | W | 8 |
| PMC0 | 0x02 | R/W | 8/1 |
| P1 | 0x08 | R/W | 8 |
| PM1 | 0x09 | W | 8/1 |
| PMC1 | 0x0A | R/W | 8 |
| P2 | 0x10 | R/W | 8/1 |
| PM2 | 0x11 | W | 8 |
| PMC2 | 0x12 | R/W | 8/1 |

After power-on/reset, I/O pins default to various configurations. The initialization routine provided by TERN libraries reconfigures some of these pins as needed for specific on-board usage as well. These configurations, as well as the processor-internal peripheral usage configurations, are listed below in Table 3.3.

| Port I/O | PMC _n = 1 | PMC _n = 0 | | Status after ve_init() | V25-Engine Location/Function |
|----------|----------------------|----------------------|---------------------|------------------------|---|
| | PM = X | PM _n = 1 | PM _n = 0 | | |
| P00 | - | Input | Output | Input | EEPROM (U7 pin 6) clock SCL |
| P01 | - | Input | Output | Input | EEPROM (U7 pin 5) data SDA |
| P02 | - | Input | Output | Input | J2 pin 4, Step 2 jumper |
| P03 | - | Input | Output | Output | J6 pin 2. HWD (hit watchdog) |
| P04 | - | Input | Output | Input | J2 pin 36 |
| P05 | - | Input | Output | Output | J2 pin 5, LED control |
| P06 | - | Input | Output | Input | J2 pin 3 |
| P07 | CLKOUT | Input | Output | CLKOUT | J1 pin 4 |
| P10 | - | /NMI | - | /NMI | J2 pin 7 |
| P11 | - | /INTP0 | - | /INTP0 | J2 pin 8, UART interrupt (if installed) |
| P12 | - | /INTP1 | - | /INTP1 | J2 pin 6 |
| P13 | /INTAK | /INTP2 | - | /INTP2 | J2 pin 33 |
| P14 | INT | /POLL | Output | Output | J2 pin 31 |
| P15 | TOUT | Input | Output | Input | J2 pin 29 |
| P16 | /SCK0 | Input | Output | Output | J2 pin 27 |
| P17 | READY | Input | Output | READY | J1 pin 27 |
| P20 | DMARQ0 | Input | Output | Input | J2 pin 30 |

| Port I/O | PMC _n = 1 | PMC _n = 0 | | Status after ve_init() | V25-Engine Location/Function |
|-------------|----------------------|----------------------|---------------------|---------------------------|---------------------------------|
| | PM = X | PM _n = 1 | PM _n = 0 | | |
| P21 | /DMAAK0 | Input | Output | Input | J2 pin 22 |
| P22 | /TC0 | Input | Output | Input | J2 pin 38 |
| P23 | DMARQ1 | Input | Output | Output | J2 pin 24 |
| P24 | /DMAAK1 | Input | Output | Input | J2 pin 20 |
| P25 | /TC1 | Input | Output | Input | J2 pin 18 |
| P26 | /HLDAK | Input | Output | Input | J2 pin 14 |
| P27 | HLDRQ | Input | Output | Input | J2 pin 12 |

Table 3.3 I/O pin default configuration

V25-Engine I/O initialization in `ve_init()` is listed below:

```
pokeb(0xffff0,0x02,0x80); /* Set PMC0 P07=CLK */
pokeb(0xffff0,0x01,0xd7); /* Set PM0 for input, P05=LED P03=HWD output */
pokeb(0xffff0,0x0a,0x80); /* Set PMC1 P17 for READY */
pokeb(0xffff0,0x09,0xaf); /* Set PM1 for input, P14=RTS1,P16=RTS0 OUTPUT */
pokeb(0xffff0,0x12,0x00); /* Set P20-P27 for port mode */
pokeb(0xffff0,0x11,0xf7); /* Set PM2 for input, P23=EN485 output */
```

The C function in the library `ve_lib` can be used to initialize PIO pins.

```
void port_init(char p, unsigned char pmc, unsigned char pm);
```

Where `p` = port 0, 1 or 2.

`pmc` = define each pin as CONTROL or I/O (0 = I/O; 1 = CONTROL).

`pm` = define each I/O pin as input or output (0 = output; 1 = input).

3.3.2 Port T Comparator Inport

Port T is an 8-bit input port whose threshold voltage can be changed in 16 steps. Each Port T input is compared with the selected threshold voltage (V_{th}). $PT_n > V_{th}$ results in a value 1, $PT_n < V_{th}$ results in a value 0. All eight results from PT0 to PT7 are latched to the port T input latches.

The resulting 8-bit latch can be accessed by the function `portt_rd(void)`, which returns the 8-bit result. V_{th} can be changed by the function `portt_wr(char vref)`. The variable `vref` {0 .. 15} sets the reference voltage by the following equation: Reference = $V_{th} * vref/16$. `vref` = 0 sets Reference = V_{th} . V_{th} is connected to a 10 K pullup resistor network and $V_{th} \approx 3.57V$. PT0 – PT6 are on J2. PT0 – PT2 are pulled up by 10 K resistors.

3.4 I/O Mapped Devices

3.4.1 I/O Space

External I/O devices use I/O mapping. You may access I/O with `inportb(port)` or `outportb(port,dat)`. The external I/O space is 64K, ranging from 0x0000 to 0xffff. In the I/O space of 0x0000-0x7fff, the I/O access time is 500 ns. In the I/O space of 0x8000-0xffff, the I/O access time is 250 ns. Table 3.4 shows more information on I/O mapped devices.

| I/O space | time (ns) | Decodes | Usage |
|---------------|-----------|--------------------------------|-----------|
| 0x0010-0x7fff | >500 ns | /IOR*/A15*addr+/IOWR*/A15*addr | USER |
| 0x8000-0xbfff | >250 ns | /IOSTB*A15*/A14 | RTC |
| 0xc000-0xffff | >250 ns | /IOSTB*A15*A14 | E=SCC J11 |

Table 3.4 I/O Mapped devices

If A15 is not used for decoding, the J2 pin 10 = E signal may be used instead:

$$/select_low = IORD*/E*lower_addr + IOWR*/E*lower_addr$$

A simple decoding circuit for interfacing to an 82C55 parallel I/O chip is shown in Figure 3.1. You can read/write to the 82C55 with *inportb(0x4020)/outportb(0x4020,dat)*.

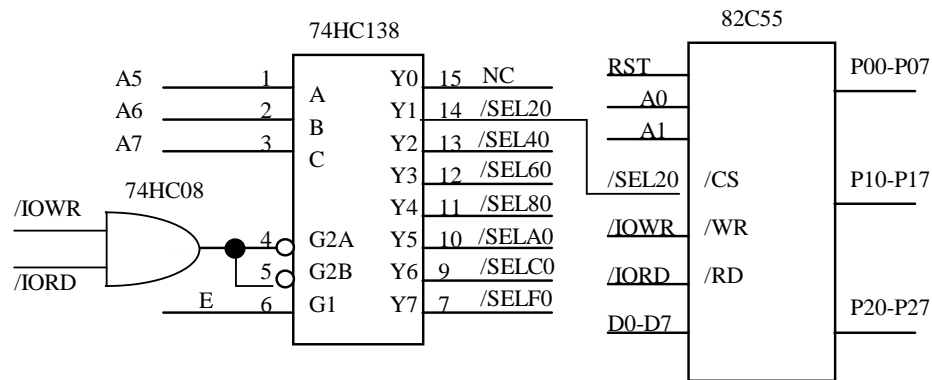


Figure 3.1 Interface the V25-Engine to external I/O devices

3.4.2 Real-time Clock RTC72423

If installed, a real-time clock RTC72423 (EPSON, U4) is mapped in the I/O address space 0x0600. It must be backed up with a lithium coin battery. The RTC is accessed via software drivers *rtc_init()* or *rtc_rd()* (see Appendix D and the Software chapter for details).

It is also possible to configure the real-time clock to raise an output line attached to an external interrupt, at 1/64 second, 1 second, 1 minute, or 1 hour intervals. This can be used in a time-driven application, or the **VOFF** signal can be used to turn on/off the controller using an external switching power supply. An example of a program showing a similar application can be found in *tern\v25\samples\ve\poweroff.c*.

3.4.3 UART SCC2691

The UART SCC2691 (Signetics, U8) is mapped in the I/O address space 0xc000-0xffff. The SCC2691 offers the following:

- a full-duplex asynchronous receiver/transmitter
- a quadruple buffered receiver data register
- an interrupt control mechanism
- programmable data format
- selectable baud rate for the receiver and transmitter
- a multi-functional and programmable 16-bit counter/timer
- an on-chip crystal oscillator
- a multi-purpose input/output, including RTS and CTS mechanism

For more information, refer to Appendix C. The SCC2691 on the V25-Engine may be used as a network 9th-bit UART. J1 pins 5 (RxD) and 7 (TxD) on the V25-Engine must be connected with H3 pins 3 and 2 on

the VE232 (see Figure 3.2). Use J1 pin 3 (RS485-) and pin 4 (RS485+) on the VE232 to join the multi-drop RS485 twisted-pair network. MPO and MPI are routed to H2.

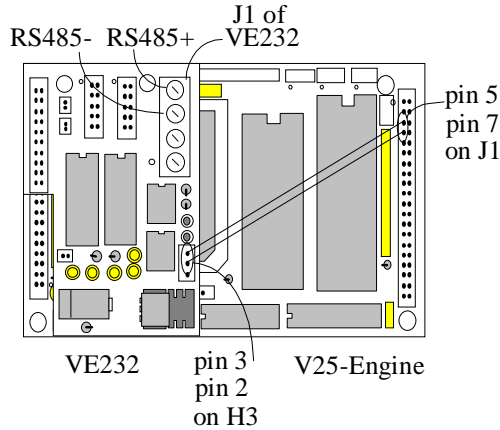


Figure 3.2 Settings and connections for networking with SCC2691 UART

3.5 I/O lines available for i386-Engine-P

Some I/O lines are used by the C-Engine™ system as listed below:

| | | |
|------|-----------|---|
| P00 | I/O | EEPROM (U7 pin 6) clock SCL |
| P01 | I/O | EEPROM (U7 pin 5) data SDA |
| P02 | I/O | J2 pin 4. If low, jump to application code which starting address is defined in the on board EEPROM (0x10 to 0x13). |
| P03* | I/O | J6 pin2. HWD (Hit watchdog) |
| P04* | I/O | WDO (Read watchdog output, U6 pin 14). |
| P05* | I/O | J2 pin 5, on board LED control |
| P06 | I/O | J2 pin 3. |
| P07 | clock out | J1 pin 4, CLKOUT, 8 MHz as system clock. |
| P10 | NMI | J10 pin 2, PFO (Power Failure Output), if J10 jumper is on. |
| P11* | INTP0 | J2 pin 8, External Interrupt Input0, falling edge effective. C-Engine™ U8 SCC2691 UART interrupt. |
| P12 | INTP1 | J2 pin 6, External Interrupt Input1, falling edge effective. |
| P13 | INTP2 | J2 pin 33, External Interrupt Input2, falling edge effective. |
| P14* | I/O | J2 pin 31, may be used as RTS1 for SER1. |
| P15 | I/O | J2 pin 29. |
| P16* | I/O | J2 pin 27, may be used as RTS0 for SER0. |
| P17 | RDY | J1 pin 27, V25 ready signal, used for more wait states. |
| P20 | I/O(DR0) | J2 pin 30, counter 0/DMA channel 0 request, rising edge active. |
| P21 | I/O(DA0) | J9 pin 1, DMA channel 0 Ack, active low, if J9 jumper on. |
| P22 | I/O | J2 pin 38. |
| P23 | I/O | J2 pin 24, counter 1/DMA1/EN485 for SCC RS485 driver. |
| P24 | I/O | J2 pin 20 and ADC SCLK. |
| P25 | I/O | J2 pin 18 and ADC DIN. |
| P26 | I/O | J2 pin 14 and ADC DOUT. |
| P27 | I/O | J2 pin 12 and ADC /CS. |
| PT0 | INPUT | J2 pin 23. |
| PT1 | INPUT | J2 pin 21. |

| | | |
|------|-------|--|
| PT2 | INPUT | J2 pin 19. |
| PT3 | INPUT | J2 pin 17. |
| PT4 | INPUT | J2 pin 15. |
| PT5 | INPUT | J2 pin 13. |
| PT6 | INPUT | J2 pin 11. |
| PT7* | INPUT | J1 pin 11, PFI (Power Failure Input, if PFI<1.3V, reset) |

3.6 Other Devices

A number of other devices are also available on the V25-Engine. Some of these are optional, and might not be installed on the particular controller you are using. For a discussion regarding the software interfaces for these components, please see the Software chapter.

3.6.1 On-board Supervisor with Watchdog Timer

The MAX691/LTC691 (U6) is a supervisor chip. With it installed, the V25-Engine has several functions that significantly improve system reliability:

- watchdog timer
- power-failure warning
- battery backup
- power-on-reset delay
- power-supply monitoring

Watchdog Timer

The watchdog timer is activated by setting a jumper on J6 of the V25-Engine. The watchdog timer provides a means of verifying proper software execution. In the user's application program, calls to the function `hitwd()` (a routine that toggles the P03=HWD pin of the MAX691) should be arranged such that the HWD pin is accessed at least once every 1.6 seconds. If the J6 jumper is on and the HWD pin is not accessed within this time-out period, the watchdog timer pulls the WDO pin low, which asserts /RESET. This automatic assertion of /RESET may recover the application program if something is wrong. After the V25-Engine is reset, WDO remains low until a transition occurs at the WDI pin of the MAX691. When controllers are shipped from the factory the J6 jumper is off, which disables the watchdog timer.

Power-failure Warning

The supervisor supports power-failure warning and backup battery protection. When power failure is sensed by the PFI pin of the MAX691 (lower than 1.3 V), the PFO is low. You may design an NMI service routine to take protect actions before the +5V drops and the processor dies. You can also measure the PFI voltage with one of the 12-bit ADC inputs. The following circuit (Figure 3.3) shows how you might use the power-failure detection logic within your application.

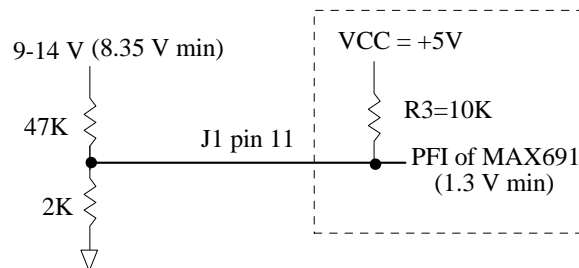


Figure 3.3 Using the supervisor chip for power failure detection

Battery Backup Protection

The backup battery protection protects data stored in the SRAM and RTC. The battery-switch-over circuit compares VCC to VBAT (+3 V lithium battery positive pin), and connects whichever is higher to VRAM

(power for SRAM and RTC). Thus, the SRAM and the real-time clock RTC72423 are backed up. In normal use, the lithium battery should last about 3-5 years without external power being supplied. When the external power is on, the battery-switch-over circuit will select the VCC to connect to the VRAM.

NOTE: When there is no battery on the V25-Engine, the VBAT signal should be shorted to ground.

3.6.2 EEPROM

A serial EEPROM of 128 bytes (24C01), 512 bytes (24C04), or 2K bytes (24C16) can be installed in U7. The V25-Engine uses the P00=SCL (serial clock) and P01=SDA (serial data) to interface with the EEPROM. The EEPROM can be used to store important data such as a node address, calibration coefficients, and configuration codes. It typically has 1,000,000 erase/write cycles, and the data retention is more than 40 years. EEPROM can be read and written to by simply calling the functions `ee_rd()` and `ee_wr()`.

3.7 12-bit ADC (TLC2543)

The TLC2543 is a 12-bit, switched-capacitor, successive-approximation, 11 channels, serial interface, analog-to-digital converter. It has three control inputs (/CS=P27; CLK=P24; DIN=P25) and is designed for communication with a host through a serial tri-state output (DOUT=P26). If P27 is low, the TLC2543 will have output on P26. If P27 is high, the TLC2543 is disabled and P24, P25, P26 are free. P27 is pulled high by a 10K resistor on board. The TLC2543 has an on-chip 14 channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC=P13) output goes high to indicate that conversion is complete. TLC2543 features differential high-impedance inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range. The analog input signal source impedance should be less than 50Ω and capable of slewing the analog input voltage into a 60 pF capacitor.

In order to operate the TLC2543, 5 V25 I/O lines are used as listed below:

| | |
|------|--|
| /CS | Chip select = P27, high to low transition enables DOUT, DIN and CLK. low to high transition disables DOUT, DIN and CLK. |
| DIN | P25, serial data input |
| DOUT | P26, 3-state serial data output. |
| EOC | P13, End of Conversion, high indicates conversion complete and data is ready |
| CLK | I/O clock = P24 |
| REF+ | Upper reference voltage (normally VCC) |
| REF- | Lower reference voltage (normally GND) |
| VCC | Power supply, +5 V input |
| GND | Ground |

The analog inputs AD0 to AD10 are available at J8 connector. REF+, GND, VCC are available at H1.

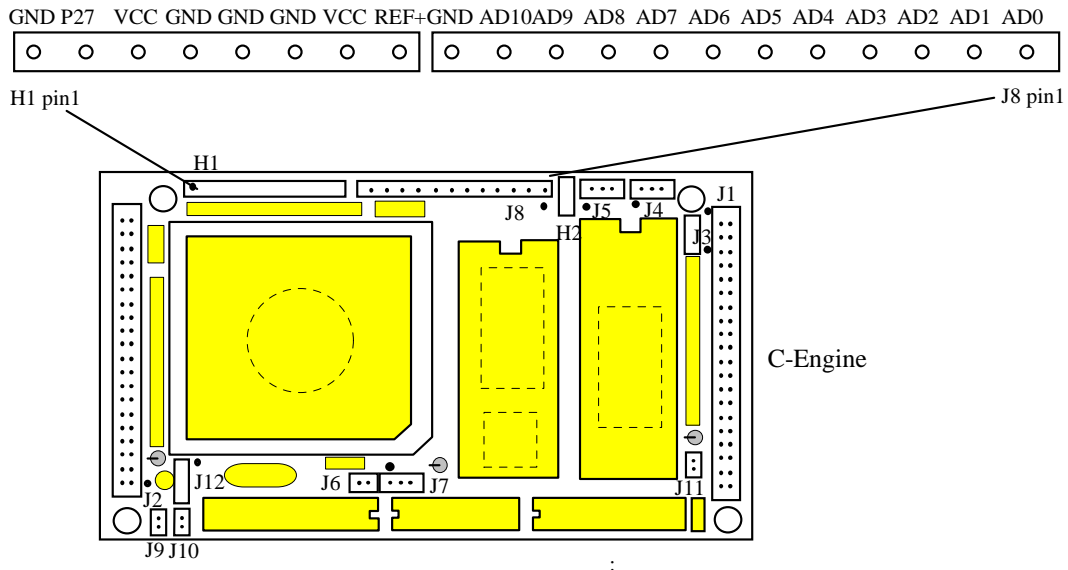


Figure 3.4 H1 and J8

3.8 Headers and Connectors

3.8.1 Expansion Headers J1 and J2

There are two 20x2 0.1 spacing headers for V25-Engine expansion: J1 and J2. Most signals are directly routed to the NEC V25 processor. These signals are 5V only, and any out-of-range voltages will most likely damage the board.

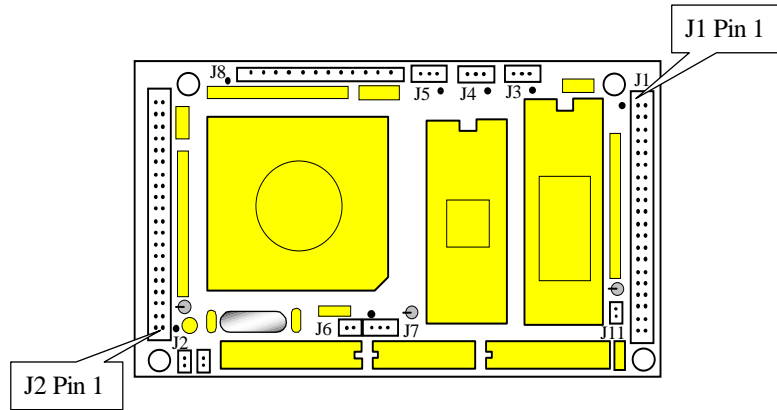


Figure 3.5 Pin 1 locations for J1 and J2

| <i>J1 Signal</i> | | | | <i>J2 Signal</i> | | | |
|------------------|----|----|-----|------------------|----|----|-------|
| VCC | 1 | 2 | GND | GND | 40 | 39 | VCC |
| MPO | 3 | 4 | CLK | P22 | 38 | 37 | /MREQ |
| RxD | 5 | 6 | GND | P04 | 36 | 35 | HWD |
| TxD | 7 | 8 | D0 | TxD0 | 34 | 33 | P13 |
| VOFF | 9 | 10 | D1 | RxD0 | 32 | 31 | P14 |
| PFI | 11 | 12 | D2 | /DR0 | 30 | 29 | P15 |
| GND | 13 | 14 | D3 | TxD1 | 28 | 27 | P16 |
| /RST | 15 | 16 | D4 | RxD1 | 26 | 25 | GND |
| RST | 17 | 18 | D5 | P23 | 24 | 23 | PT0 |
| /IOSTB | 19 | 20 | D6 | P21 | 22 | 21 | PT1 |
| MPI | 21 | 22 | D7 | P24 | 20 | 19 | PT2 |
| /MSTB | 23 | 24 | GND | P25 | 18 | 17 | PT3 |
| GND | 25 | 26 | A7 | R/W | 16 | 15 | PT4 |
| RDY | 27 | 28 | A6 | P26 | 14 | 13 | PT5 |
| /IOWR | 29 | 30 | A5 | P27 | 12 | 11 | PT6 |
| /IORD | 31 | 32 | A4 | E | 10 | 9 | Vth |
| VRAM | 33 | 34 | A3 | P11 | 8 | 7 | /NMI |
| VBAT | 35 | 36 | A2 | P12 | 6 | 5 | P05 |
| GND | 37 | 38 | A1 | P02 | 4 | 3 | P06 |
| VCC | 39 | 40 | A0 | GND | 2 | 1 | GND |

Table 3.5 Signals for J1 and J2, 20x2 expansion ports

Signal definitions for J1:

| | |
|--------|--|
| VCC | +5V power supply |
| GND | Ground |
| CLK | NEC V25 pin 12, system clock |
| RxD | data receive of UART SCC2691, U8 |
| TxD | data transmit of UART SCC2691, U8 |
| MPO | Multi-Purpose Output of SCC2691, U8 |
| MPI | Multi-Purpose Input of SCC2691, U8 |
| VOFF | real-time clock output of RTC72423 U4 |
| D0-D7 | NEC V25 8-bit external data lines |
| A0-A7 | NEC V25 address lines |
| PFI | power failure input signal of MAX691 |
| /RST | reset signal, active low |
| RST | reset signal, active high |
| /IORD | Expansion I/O Read |
| /IOWR | Expansion I/O Write |
| /MSTB | NEC V25 pin 84. Memory bus cycle has started |
| /IOSTB | NEC V25 pin 1. I/O read or write strobe output |
| RDY | Ready input |
| VBAT | +3V lithium battery positive pin |
| VRAM | power for backing up SRAM and RTC |

Signal definitions for J2:

| | |
|--------|---|
| VCC | +5V power supply, < 200 mA |
| GND | Ground |
| Pxx | NEC V25 Port I/O pins |
| R/W | NEC V25 pin 83 |
| TxD0 | NEC V25 pin 44, transmit data of serial channel 0 |
| RxD0 | NEC V25 pin 41, receive data of serial channel 0 |
| TxD1 | NEC V25 pin 47, transmit data of serial channel 1 |
| RxD1 | NEC V25 pin 45, receive data of serial channel 1 |
| PT 0-7 | Port T Inputs |
| /MREQ | NEC V25 pin 2 |
| HWD | Hit Watchdog |

3.8.2 Jumpers

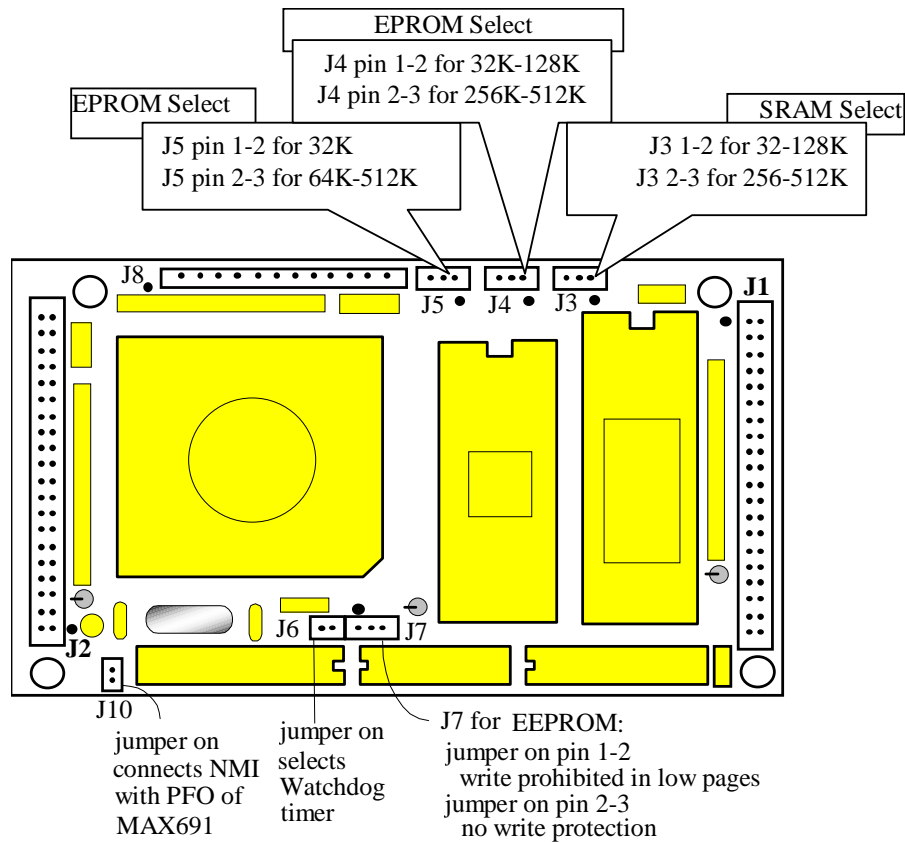


Figure 3.5 Jumper/Headers on the V25-Engine

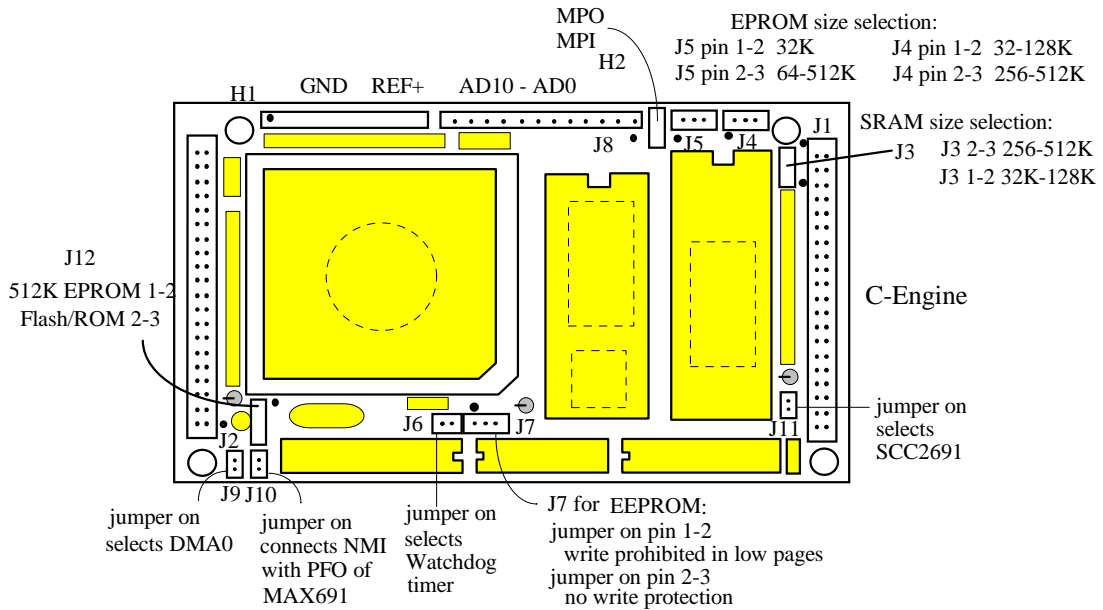


Figure 3.6 Jumper settings on C-Engine™

The following table lists the jumpers and connectors on the V25-Engine:

| Name | Size | Function | Possible Configuration |
|------|------|---------------------------|---|
| J1 | 20x2 | main expansion port | |
| J2 | 20x2 | main expansion port | |
| J3 | 3x1 | SRAM selection: | pin 2-3: SRAM 256KB-512KB pin 1-2: SRAM 32KB-128KB |
| J4 | 3x1 | ROM/Flash size selection: | pin 1-2: ROM or Flash size 32KB-128KB pin 2-3: ROM or Flash size 256KB-512KB |
| J5 | 3x1 | ROM 512KB selection: | pin 1-2: ROM size 512KB pin 2-3: Flash 128KB-512KB, or ROM < 512 KB |
| J6 | 2x1 | Watchdog Timer | Jumper on = WD enabled else disabled |
| J7 | 3x1 | EEPROM Write Protection | pin 1-2: EEPROM write prohibited in low pages. pin 2-3: No EEPROM write protection. |
| J8 | 12x1 | High address lines | A8 – A19 |
| J10 | 2x1 | Power Fail Int and /NMI | Pin 1 = /PFO, pin 2 = /NMI. If jumper is on, when a power failure is sensed /PFO will generate interrupt on /NMI. |

The following table lists the jumpers and connectors on the C-Engine:

| Name | Size | Function | Possible Configuration |
|------|------|---------------------------|---|
| J1 | 20x2 | main expansion port | |
| J2 | 20x2 | main expansion port | |
| J3 | 3x1 | SRAM selection: | pin 2-3: SRAM 256KB-512KB pin 1-2: SRAM 32KB-128KB |
| J4 | 3x1 | ROM/Flash size selection: | pin 1-2: ROM or Flash size 32KB-128KB pin 2-3: ROM or Flash size 256KB-512KB |

| Name | Size | Function | Possible Configuration |
|------|------|-------------------------|---|
| J5 | 3x1 | EPROM size selection | pin 1-2: EPROM size 32K pin 2-3: EPROM size 64K-512K |
| J6 | 2x1 | Watchdog Timer | Jumper on = WD enabled. Jumper off = disabled |
| J7 | 3x1 | EEPROM Write Protection | pin 1-2: EEPROM write prohibited in low pages. pin 2-3: No EEPROM write protection. |
| J8 | 12x1 | High Address Lines | ADO-10, 11 Channels of analog inputs |
| J10 | 2x1 | Power Fail Int and /NMI | Pin 1 = /PFO, pin 2 = /NMI. If jumper is on, when a power failure is sensed /PFO will generate interrupt on /NMI. |
| J11 | 2x1 | Select SCC2691 UART | A jumper must be put on this connector to select SCC2691 UART |
| J12 | 3x1 | EPROM size selection | pin 1-2: 512K EPROM pin 2-3: 32K-256K EPROM/EEPROM |
| H1 | 8x1 | | REF+, VCC, GND, P27(LTC2543 ADC CS) |
| H2 | 2x1 | | UART SCC2691 MPO and MPI |
| J15 | 2x1 | | pin 1: REF+ pin 2: VCC J15 is located next to TLC2543 pin 14 and pin 15. |

A wire jumper may be soldered on the back side (solder side) of the C-Engine™ connecting REF+=VCC. If you want to provide your reference voltage for the ADC, you need to cut off that wire and provide your reference from J8 connector.

Chapter 4: Software

Please refer to the Technical Manual of the “C/C++ Development Kit for TERN 16-bit Embedded Microcontrollers” for details on debugging and programming tools.

For details regarding software function prototypes and sample files demonstrating their use, please refer to the Software Glossary in Appendix F.

Guidelines, awareness, and problems in an interrupt driven environment

Although the C/C++ Development Kit provides a simple, low cost solution to application engineers, some guidelines must be followed. If they are not followed, you may experience system crashes, PC hang-ups, and other problems.

The debugging of interrupt handlers with the Remote Debugger can be a challenge. It is possible to debug an interrupt handler, but there is a risk of experiencing problems. Most problems occur in multi-interrupt-driven situations. Because the remote kernel running on the controller is interrupt-driven, it demands interrupt services from the CPU. If an application program enables interrupt and occupies the interrupt controller for longer than the remote debugger can accept, the debugger will time-out. As a result, your PC may hang-up. In extreme cases, a power reset may be required to restart your PC.

For your reference, be aware that our system is remote kernel interrupt-driven for debugging.

The run-time environment on TERN controllers consists of an I/O address space and a memory address space. I/O address space ranges from **0x0000** to **0xffff**, or 64 KB. Memory address space ranges from **0x00000** to **0xfffff** in real-mode, or 1 MB. These are accessed differently, and not all addresses can be translated and handled correctly by hardware. I/O and memory mappings are done in software to define how translations are implemented by the hardware. Implicit accesses to I/O and memory address space occur throughout your program from TERN libraries as well as simple memory accesses to either code or global and stack data. You can, however, explicitly access any address in I/O or memory space, and you will probably need to do so in order to access processor registers and on-board peripheral components (which often reside in I/O space) or non-mapped memory.

This is done with four different sets of similar functions, described below.

poke/pokeb

Arguments: unsigned int segment, unsigned int offset, unsigned int/unsigned char data

Return value: none

These standard C functions are used to place specified data at any memory space location. The **segment** argument is left shifted by four and added to the **offset** argument to indicate the 20-bit address within memory space. **poke** is used for writing 16 bits at a time, and **pokeb** is used for writing 8 bits.

The process of placing data into memory space means that the appropriate address and data are placed on the address and data-bus, and any memory-space mappings in place for this particular range of memory will be used to activate appropriate chip-select lines and the corresponding hardware component responsible for handling this data.

peek/peekb**Arguments:** unsigned int segment, unsigned int offset**Return value:** unsigned int/unsigned char data

These functions retrieve the data for a specified address in memory space. Once again, the **segment** address is shifted left by four bits and added to the **offset** to find the 20-bit address. This address is then output over the address bus, and the hardware component mapped to that address should return either an 8-bit value or a 16-bit value over the data bus. If there is no component mapped to that address, this function will return random garbage values every time you try to peek into that address.

outport/outportb**Arguments:** unsigned int address, unsigned int/unsigned char data**Return value:** none

This function is used to place the **data** into the appropriate **address** in I/O space. It is used most often when working with processor registers that are mapped into I/O space and must be accessed using either one of these functions. This is also the function used in most cases when dealing with user-configured peripheral components.

When dealing with processor registers, be sure to use the correct function. Use **outport** if you are dealing with a 16-bit register.

inport/inportb**Arguments:** unsigned int address**Return value:** unsigned int/unsigned char data

This function can be used to retrieve data from components in I/O space. You will find that most hardware options added to TERN controllers are mapped into I/O space, since memory space is valuable and is reserved for uses related to the code and data. Using I/O mappings, the address is output over the address bus, and the returned 16 or 8-bit value is the return value.

For a further discussion of I/O and memory mappings, please refer to the Hardware chapter of this technical manual.

4.1 VE.LIB

VE.LIB is a C library for basic V25-Engine operations. It includes the following modules: VE.OBJ, SER0.OBJ, SER1.OBJ, SCC.OBJ, and VEEE.OBJ. You need to link VE.LIB in your applications and include the corresponding header files. The following is a list of the header files:

| Include-file name | Description |
|-------------------|--|
| VE.H | PPI, timer/counter, ADC, DAC, RTC, Watchdog, |
| SER0.H | Internal serial port 0 |
| SER1.H | Internal serial port 1 |
| SCC.H | External UART SCC2691 |
| VEEE.H | on-board EEPROM |

4.2 Functions in VE.OBJ

4.2.1 V25-Engine Initialization

VE_init

This function should be called at the beginning of every program running on V25-Engine core controllers. It provides default initialization and configuration of the various I/O pins, interrupt vectors, sets up expanded DOS I/O, and provides other processor-specific updates needed at the beginning of every program.

ve_init will initialize the I/O pin functions and store the initial register control bytes into the EEPROM (see Appendix E). You may use these image registers to determine the status of the port but you must update these registers in your applications. The port0-2 are initialized as shown below:

```
void ve_init(void){
    pokeb(0xffff,0x02,0x80); /* Set PMC0 P07=CLK */
    pokeb(0xffff,0x01,0xd7); /* Set PM0 for input, P05=LED P03=HWD output */
    pokeb(0xffff,0x0a,0x80); /* Set PMC1 P17 for READY */
    pokeb(0xffff,0x09,0xaf); /* Set PM1 for input, P14=RTS1,P16=RTS0 OUTPUT */
    pokeb(0xffff,0x12,0x00); /* Set P20-P27 for port mode */
}
```

4.2.2 External Interrupt Initialization

There are up to five external interrupt sources on the V25-Engine, consisting of four maskable interrupt pins (**INTP2-INTP0**, **INT**) and one non-maskable interrupt (**NMI**). There are also additional internal interrupt sources not connected to the external pins, consisting of two timers, a time base counter, two DMA channels, both asynchronous serial ports, and the **NMI** from the watchdog timer. For a detailed discussion involving the interrupts, the user should refer to chapter 4 of the NEC V25 CPU User's Manual.

TERN provides functions to enable/disable all of the external interrupts. The user can call any of the interrupt init functions listed below for this purpose. The first argument indicates whether the particular interrupt should be enabled, and the second is a function pointer to an appropriate interrupt service routine that should be used to handle the interrupt. The TERN libraries will set up the interrupt vectors correctly for the specified external interrupt line.

At the end of interrupt handlers, the user should run a finish interrupt routine. This can be done using the *fint()* function.

void intpx_init

Arguments: unsigned char i, void interrupt far(* intpx_isr) ())

Return value: none

These functions can be used to initialize any one of the external interrupt channels (for pin locations and other physical hardware details, see the Hardware chapter). The first argument **i** indicates whether this particular interrupt should be enabled or disabled. The second argument is a function pointer which will act as the interrupt service routine.

By default, the interrupts are all disabled after initialization. To disable them again, you can repeat the call but pass in 0 as the first argument.

The NMI (Non-Maskable Interrupt) is special in that it can not be masked (disabled). The default ISR will return on interrupt.

```
void nmi_init(void);
void intp0_init( unsigned char i, void interrupt far(* int0_isr)() );
void intp1_init( unsigned char i, void interrupt far(* int1_isr)() );
```

```
void intp2_init( unsigned char i, void interrupt far(* int2_isr)() );
void timer0_init(unsigned char i, void interrupt far(* timer0_isr)());
void timer1_init(unsigned char i, void interrupt far(* timer1_isr)());
void timer2_init(unsigned char i, void interrupt far(* timer2_isr)());
void time_base_init(char i, void interrupt far(*time_base_isr)());
```

4.2.3 I/O Initialization

There are two ports of 16 I/O pins available on the V25-Engine. Hardware details regarding these PIO lines can be found in the Hardware chapter.

There are several functions provided for access to the PIO lines. At the beginning of any application where you choose to use the PIO pins as input/output, you will probably need to initialize these pins in one of the four available modes. Before selecting pins for this purpose, make sure that the peripheral mode operation of the pin is not needed for a different use within the same application.

You should also confirm the PIO usage that is described above within `ve_init()`. During initialization, several lines are reserved for TERN usage and you should understand that these are not available for your application. There are several PIO lines that are used for other on-board purposes. These are all described in some detail in the Hardware chapter of this technical manual. For a detailed discussion of the I/O ports, please refer to chapter 7 of the NEC V25 User's Manual.

Please see the sample program `portx.c` in `tern\v25\samples\ve`. You will also find that these functions are used throughout TERN sample files, as most applications do find it necessary to re-configure the PIO lines.

The functions `port_wr` and `port_rd` can be quite slow when accessing the Port I/O pins. The maximum efficiency you can get from the Port I/O pins occurs if you modify the Port registers directly with an `outport` instruction instead of using `port_wr/port_rd`.

See the Hardware chapter for Port register addresses.

void port_init

Arguments: char p, unsigned char pmc, unsigned char pm

Return value: none

p refers to Port 0, Port 1 or Port2.

pmc refers to the 8-bit *port mode control* register value for port **p**.

- A '0' bit sets the pin to I/O mode
- A '1' bit sets the pin to CONTROL mode

pm refers to the 8-bit *port mode* register value for port **p**. This register is valid for pins only I/O mode pins.

- A '0' bit sets the pin to output
- A '1' bit sets the pin to input

char port_rd

Arguments: char p

Return value: byte indicating Port I/O status for port p.

Each bit of the returned 8-bit value indicates the current I/O value for the Port I/O pins in port **p**.

void pio_wr

Arguments: char p, char dat

Return value: none

Writes an 8-bit value to port **p**. Only changes status of I/O mode output pins.

Example 4.1 Set port 0 as I/O, bits 0 – 3 as input, 4 – 7 as output.

```
port_init(0, 0x00, 0xf0);
p = Port 0,
pmc = 0 (I/O),
pm 0-3 = 1, pm 4-7 = 0.
```

Example 4.2 Set pins 20 and 23 as DMA Request. All other port 2 pins as output.

```
port_init(2, 0x09, 0x00);
p = Port 2,
pmc = bit 0 and 3 = 1 (Control), all others = 0 (I/O)
pm = all 0s. Since pins 20 and 23 are control functions, the pm field is not
relevant.
```

In most cases it is only necessary to change the value of one or two pins in the port data register. Since the port data register is a read/write register, it is possible to mask the pins that do not need to change. In this case, the *port_init* function cannot be used. Instead, the port data register can be directly accessed using the *poke* and *peek* functions.

Example 4.3 Using bitwise OR to set a single bit high, set pin 23 high without modifying the other pins. Assume all port 2 is output and that all pins are low.

```
pokeb(0xffff, 0x10, (unsigned char) (peekb( 0xffff, 0x10) | 0x08) );
```

Assuming that all of port 2 is outputting low, the *peekb* function will return a value of *0x00*. A bitwise ‘OR’ with the value *0x00* and the mask *0x08* equals *0x08*. Port 2 now outputs *0x08*.

Example 4.4 Using bitwise AND to reset a single bit low, set pin 23 low without modifying the other pins. Assume settings are the same after executing Example 4.3.

```
pokeb(0xffff, 0x10, (unsigned char) (peekb( 0xffff, 0x10) & 0xF7) );
```

Assuming the settings from Example 4.3 are still present, the *peekb* function should return a value of *0x08*. A bitwise ‘AND’ with the value *0x08* and the mask *0xF7* equals *0x00*. Port is again set to *0x00* (all pins low).

While the port data registers are read/write registers, the port control registers *pmc* and *pm* are not. Modifying only certain pins in these registers requires the use of global variables to store the values of these registers. This means that any changes to the *pmc* or *pm* registers must be accounted for in the global variable. As in the previous example, the bitwise OR and AND expressions can be used to mask the register bits.

Example 4.5 Set port 2 pins 0 through 3 as output.

```
// The following global variable defines the pm2 register
unsigned char pm2;

/* assume pm2 has been correctly maintained. The following code will modify the pm2
   register such that bits 0 through 3 are low. Use AND to set bits low */

pokeb(0xffff0, 0x11, ( pm2 = ( pm2 & 0xF0 ) ) ); //pm2 must be set to a new register
   value
```

Example 4.6 Set port 2 pins 0 through 3 as input.

```
// The following global variable defines the pm2 register
unsigned char pm2;

/* assume pm2 has been correctly maintained. The following code will modify the pm2
   register such that bits 0 through 3 are high. Use OR to set bits high */

pokeb(0xffff0, 0x11, ( pm2 = ( pm2 | 0x0F ) ) ); //pm2 must be set to new register value
```

4.2.4 Port T

Port T is an 8-bit input port whose threshold voltage can be changed in 16 steps. Comparator operation is performed through this port. Each Port T input is compared with the selected threshold voltage (V_{th}). $PT_n > V_{th}$ results in a value 1, $PT_n < V_{th}$ results in a value 0. All eight results from PT0 to PT7 are latched to the port T input latches.

The resulting 8-bit latch can be accessed by the function `portt_rd(void)` which returns the 8-bit result. V_{th} can be changed by the function `portt_wr(char vref)`. The variable `vref` {0 .. 15} sets the reference voltage by the following equation: Reference = $V_{th} * vref/16$. `vref = 0` sets Reference = V_{th} . V_{th} is connected to a 10 K pullup resistor network and $V_{th} \approx 3.57V$. PT0 – PT6 are on J2. PT0 – PT2 are pulled up by 10k resistors.

void portt_wr(char vref)

where `vref` is a number to select VREF

| | |
|------------------------|------------|
| <code>vref = 0</code> | VTHx 1 |
| <code>vref = 1</code> | VTHx 1/16 |
| <code>vref = 2</code> | VTHx 2/16 |
| <code>vref = 3</code> | VTHx 3/16 |
| <code>vref = 4</code> | VTHx 4/16 |
| <code>vref = 5</code> | VTHx 5/16 |
| <code>vref = 6</code> | VTHx 6/16 |
| <code>vref = 7</code> | VTHx 7/16 |
| <code>vref = 8</code> | VTHx 8/16 |
| <code>vref = 9</code> | VTHx 9/16 |
| <code>vref = 10</code> | VTHx 10/16 |
| <code>vref = 11</code> | VTHx 11/16 |
| <code>vref = 12</code> | VTHx 12/16 |
| <code>vref = 13</code> | VTHx 13/16 |
| <code>vref = 14</code> | VTHx 14/16 |
| <code>vref = 15</code> | VTHx 15/16 |

```
char portt_rd(void)
```

returns an 8-bit character representing the comparator output if the voltage at PT0 < Vref, bit 0=0 else 1.

4.2.5 Timer Units

The two timers present on the V25-Engine can be used for a variety of applications. The timers run at a maximum of 1/6 of the processor clock rate, which determines the maximum resolution that can be obtained.

These timers are controlled and configured through a mode register that is specified using the software interfaces. The mode register is described in detail in chapter 9 of the NEC V25 User's Manual.

The timers can be used to time execution of your user defined code by reading the timer values before and after execution of any piece of code. For a sample file demonstrating this application, see the sample file *timer.c* in the directory *tern\v25\samples\ve*.

The specific behavior that you might want to implement is described in detail in chapter 9 of the NEC V25 User's Manual.

```
void timer0_init
```

```
void timer1_init
```

Arguments: unsigned char mode, unsigned int md0, unsigned int tm0

Return values: none

The argument **mode** is the value that you wish placed into the **TMC0/TMC1** mode registers for configuring the two timers.

The argument **md0** is the modulo timer count and **t0** is the timer count.

```
void timer0_interrupt
```

```
void timer1_interrupt
```

Arguments: unsigned char i, void interrupt far (* timer0_isr)()

Return values: none

The argument **i** enables the interrupt and (*timer0_isr)() or (*timer1_isr)() points to the interrupt service routine. The interrupt service routine is called whenever count 0 is reached, with other behavior possible depending on the value specified for the control register.

4.2.6 Other library functions

On-board supervisor MAX691 or LTC691

The watchdog timer offered by the MAX691 or LTC691 offers an excellent way to monitor improper program execution. If the watchdog timer (**J9**) jumper is set, the function **hitwd()** must be called every 1.6 seconds of program execution. If this is not executed because of a run-time error, such as an infinite loop or stalled interrupt service routine, a hardware reset will occur.

```
void hitwd
```

Arguments: none

Return value: none

Resets the supervisor timer for another 1.6 seconds.

```
void led
```

Arguments: int ledd

Return value: none

Turns the on-board LED on or off according to the value of **ledd**.

Real-Time Clock

The real-time clock can be used to keep track of real time. Backed up by a lithium-coin battery, the real time clock can be accessed and programmed using two interface functions.

The real time clock only allows storage of two digits of the year code, as reflected below. As a result, application developers should be careful to account for a roll-over in digits in the year 2000. One solution might be to store an offset value in non-volatile storage such as the EEPROM.

A common data structure is used to access and use both interfaces.

```
typedef struct{
    unsigned char sec1; One second digit.
    unsigned char sec10; Ten second digit.
    unsigned char min1; One minute digit.
    unsigned char min10; Ten minute digit.
    unsigned char hour1; One hour digit.
    unsigned char hour10; Ten hour digit.
    unsigned char day1; One day digit.
    unsigned char day10; Ten day digit.
    unsigned char mon1; One month digit.
    unsigned char mon10; Ten month digit.
    unsigned char year1; One year digit.
    unsigned char year10; Ten year digit.
    unsigned char wk; Day of the week.
} TIM;
```

int rtc_rd

Arguments: TIM *r

Return value: int error_code

This function places the current value of the real time clock within the argument **r** structure. The structure should be allocated by the user. This function returns 0 on success and returns 1 in case of error, such as the clock failing to respond.

Void rtc_init

Arguments: char* t

Return value: none

This function is used to initialize and set a value into the real-time clock. The argument **t** should be a null-terminated byte array that contains the new time value to be used.

The byte array should correspond to { *weekday, year10, year1, month10, month1, day10, day1, hour10, hour1, minute10, minute1, second10, second1, 0* }.

If, for example, the time to be initialized into the real time clock is June 5, 1998, Friday, 13:55:30, the byte array would be initialized to:

```
unsigned char t[14] = { 5, 9, 8, 0, 6, 0, 5, 1, 3, 5, 5, 3, 0 };
```

Delay

In many applications it becomes useful to pause before executing any further code. There are functions provided to make this process easy. For applications that require precision timing, you should use the hardware timers provided on-board for this purpose.

void delay0**Arguments:** unsigned int t**Return value:** none

This function is just a simple software loop. The actual time that it waits depends on processor speed as well as interrupt latency. The code is functionally identical to:

```
While(t) { t--; }
```

Passing in a t value of 600 causes a delay of approximately 1 ms.

void delay_ms**Arguments:** unsigned int**Return value:** none

This function is similar to delay0, but the passed in argument is in units of milliseconds instead of loop iterations. Again, this function is highly dependent upon the processor speed.

unsigned int crc16**Arguments:** unsigned char *wptr, unsigned int count**Return value:** unsigned int value

This function returns a simple 16-bit CRC on a byte-array of **count** size pointed to by **wptr**.

void ve_reset**Arguments:** none**Return value:** none

This function is similar to a hardware reset, and can be used if your program needs to re-start the board for any reason. Depending on the current hardware configuration, this might either start executing code from the DEBUG ROM or from some other address.

4.3 Functions in SER0.OBJ/SER1.OBJ

The functions described in this section are prototyped in the header files **ser0.h** and **ser1.h** in the **tern\v25\include** directory.

The internal asynchronous serial ports are functionally identical. SER0 is used by the DEBUG ROM provided as part of the TERN EV/DV software kits for communication with the PC. As a result, you will not be able to debug code directly written for serial port 0.

Two asynchronous serial ports are integrated in the NEC V25 CPU: SER0 and SER1. Both ports have baud rates based on the 8 MHz clock.

By default, SER0 is used by the DEBUG ROM for application download/debugging in Step One and Step Two. We will use SER1 as the example in the following discussion; any of the interface functions which are specific to SER1 can be easily changed into function calls for SER0. While selecting a serial port for use, please realize that some pins might be shared with other peripheral functions. This means that in certain limited cases, it might not be possible to use a certain serial port with other on-board controller functions. For details, you should see chapter 11 of the NEC V25 User's Manual.

TERN interface functions make it possible to use one of a number of predetermined baud rates. These baud rates are achieved by specifying a divisor for the processor frequency.

The following table shows the function arguments that express each baud rate, to be used in TERN functions.

| Function Argument | Baud Rate |
|-------------------|------------------|
| 1 | 110 |
| 2 | 150 |
| 3 | 300 |
| 4 | 600 |
| 5 | 1200 |
| 6 | 2400 |
| 7 | 4800 |
| 8 | 9600 |
| 9 | 19,200 (default) |
| 10 | 38,400 |
| 11 | 57,600 |
| 12 | 76,800 |
| 13 | 115,000 |
| 14 | 230,000 |
| 15 | 460,800 |
| 16 | 1 Meg |

Table 4.1 Baud rate values

After initialization by calling `sl_init()`, SER1 is configured as a full-duplex serial port and is ready to transmit/receive serial data at one of the specified 16 baud rates.

An input buffer, `ser1_in_buf` (whose size is specified by the user), will automatically store the receiving serial data stream into the memory by macro service operation. In terms of receiving, there is no software overhead or interrupt latency for user application programs even at the highest baud rate. Macro service transfer allows efficient handling of incoming data. The user only has to check the buffer status with `serhit1()` and take out the data from the buffer with `getser1()`, if any. The input buffer is used as a circular ring buffer, as shown in Figure 4.1. However, the transmit operation is interrupt-driven.

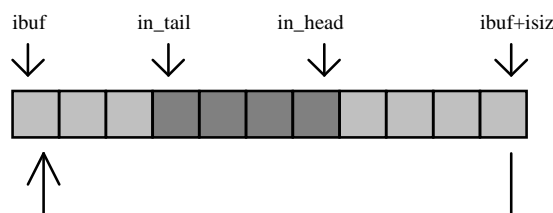


Figure 4.1 Circular ring input buffer

The input buffer (**ibuf**), buffer size (**isiz**), mode (**mode**), and baud rate (**baud**) are specified by the user with `sl_init()`. The mode is the setting value for the serial port control register. A value of `0xC9` will set the serial port in the following manner:

transmit enable, receive enable, no parity, 8 data bits, 1 stop bit

Due to the nature of high-speed baud rates and possible effects from the external environment, serial input data will automatically fill in the buffer circularly without stopping, regardless of overwrite. If the user does not take out the data from the ring buffer with `getser1()` before the ring buffer is full, new data will overwrite the old data without warning or control. Thus it is important to provide a sufficiently large buffer

if large amounts of data are transferred. For example, if you are receiving data at 9600 baud, a 4 KB buffer will be able to store data for approximately four seconds.

However, it is always important to take out data early from the input buffer, before the ring buffer rolls over. You may designate a higher baud rate for transmitting data out and a slower baud rate for receiving data. This will give you more time to do other things, without overrunning the input buffer. You can use `serhit1()` to check the status of the input buffer and return the offset of the `in_head` pointer from the `in_tail` pointer. A return value of 0 indicates no data is available in the buffer.

You can use `getser1()` to get the serial input data byte by byte using FIFO from the buffer. The `in_tail` pointer will automatically increment after every `getser1()` call. It is not necessary to suspend external devices from sending in serial data with /RTS. Only a hardware reset or `s1_close()` can stop this receiving operation.

For transmission, you can use `putser1()` to send out a byte, or use `putsers1()` to transmit a character string. You can put data into the transmit ring buffer, `s1_out_buf`, at any time using this method. The transmit ring buffer address (`obuf`) and buffer length (`osiz`) are also specified at the time of initialization. The transmit interrupt service will check the availability of data in the transmit buffer. If there is no more data (the head and tail pointers are equal), it will disable the transmit interrupt. Otherwise, it will continue to take out the data from the out buffer, and transmit. After you call `putser1()` and transmit functions, you are free to do other tasks with no additional software overhead on the transmitting operation. It will automatically send out all the data you specify. After all data has been sent, it will clear the busy flag and be ready for the next transmission.

The sample program `ser1_0.c` demonstrates how a protocol translator works. It would receive an input HEX file from SER1 and translate every ':' character to '?'. The translated HEX file is then transmitted out of SER0. This sample program can be found in `tern\186\samples\ve`.

Software Interface

Before you can use the serial ports, they must be initialized.

There is a data structure containing important serial port state information that is passed as argument to the TERN library interface functions. The **COM** structure should normally be manipulated only by TERN libraries. It is provided to make debugging of the serial communication ports more practical. Since it allows you to monitor the current value of the buffer and associated pointer values, you can watch the transmission process.

The two serial ports have similar software interfaces. Any interface that makes reference to either `s0` or `ser0` can be replaced with `s1` or `ser1`, for example. Each serial port should use its own **COM** structure, as defined in `ve.h`.

```
typedef struct {
    unsigned char ready;           /* TRUE when ready */
    unsigned char baud;
    unsigned char mode;
    unsigned char iflag;         /* interrupt status */
    unsigned char *in_buf;       /* Input buffer */
    int in_tail;                 /* Input buffer TAIL ptr */
    int in_head;                 /* Input buffer HEAD ptr */
    int in_size;                 /* Input buffer size */
    int in_crCnt;                /* Input <CR> count */
    unsigned char in_mt;         /* Input buffer FLAG */
    unsigned char in_full;       /* input buffer full */
    unsigned char *out_buf;      /* Output buffer */
    int out_tail;                /* Output buffer TAIL ptr */
    int out_head;                /* Output buffer HEAD ptr */
    int out_size;                /* Output buffer size */
    unsigned char out_full;      /* Output buffer FLAG */
    unsigned char out_mt;        /* Output buffer MT */
}
```

```

unsigned char tmso; // transmit macro service operation
unsigned char rts;
unsigned char dtr;
unsigned char en485;
unsigned char err;
unsigned char node;
unsigned char cr; /* scc CR register */
unsigned char slave;
unsigned int in_segm; /* input buffer segment */
unsigned int in_offs; /* input buffer offset */
unsigned int out_segm; /* output buffer segment */
unsigned int out_offs; /* output buffer offset */
unsigned char byte_delay; /* V25 macro service byte delay */
} COM;

```

sn_init**Arguments:** unsigned char **b**, unsigned char* **ibuf**, int **isiz**, unsigned char* **obuf**, int **osiz**, COM* **c****Return value:** none

This function initializes either SER0 or SER1 with the specified parameters. **mode** is the serial control register value. **b** is the baud rate value shown in Table 4.1. The arguments **ibuf** and **isiz** specify the input-data buffer, and **obuf** and **osiz** specify the location and size of the transmit ring buffer.

If mode = 0xc9, the serial ports are initialized for 8-bit, 1 stop bit, no parity communication.

There are a couple different functions used for transmission of data. You can actually place data within the output buffer manually, incrementing the head and tail buffer pointers appropriately. If you do not call one of the following functions, however, the driver interrupt for the appropriate serial-port will be disabled, which means that no values will be transmitted. This allows you to control when you wish the transmission of data within the outbound buffer to begin. Once the interrupts are enabled, it is dangerous to manipulate the values of the outbound buffer, as well as the values of the buffer pointer.

putsrn**Arguments:** unsigned char **outch**, COM ***c****Return value:** int **return_value**

This function places one byte **outch** into the transmit buffer for the appropriate serial port. The return value returns one in case of success, and zero in any other case.

putsersn**Arguments:** char* **str**, COM ***c****Return value:** int **return_value**

This function places a null-terminated character string into the transmit buffer. The return value returns one in case of success, and zero in any other case.

DMA transfer automatically places incoming data into the inbound buffer. **serhitn()** should be called before trying to retrieve data.

serhitn**Arguments:** COM ***c****Return value:** int **value**

This function returns 1 as **value** if there is anything present in the in-bound buffer for this serial port.

getsern**Arguments:** COM *c**Return value:** unsigned char value

This function returns the current byte from *sn_in_buf*, and increments the *in_tail* pointer. Once again, this function assumes that *serhitn* has been called, and that there is a character present in the buffer.

getsersn**Arguments:** COM c, int len, char* str**Return value:** int value

This function fills the character buffer *str* with at most *len* bytes from the input buffer. It also stops retrieving data from the buffer if a carriage return (ASCII: **0x0d**) is retrieved.

This function makes repeated calls to *getser*, and will block until *len* bytes are retrieved. The return *value* indicates the number of bytes that were placed into the buffer.

Be careful when you are using this function. The returned character string is actually a byte array terminated by a null character. This means that there might actually be multiple null characters in the byte array, and the returned *value* is the only definite indicator of the number of bytes read. Normally, we suggest that the *getsers* and *putsers* functions only be used with ASCII character strings. If you are working with byte arrays, the single-byte versions of these functions are probably more appropriate.

Miscellaneous Serial Communication Functions

One thing to be aware of in both transmission and receiving of data through the serial port is that TERN drivers only use the basic serial-port communication lines for transmitting and receiving data. Hardware flow control in the form of **CTS** (Clear-To-Send) and **RTS** (Ready-To-Send) is not implemented. There are, however, functions available that allow you to check and set the value of these I/O pins appropriately for whatever form of flow control you wish to implement. Before using these functions, you should once again be aware that the peripheral pin function you are using might not be selected as needed. For details, please refer to the NEC V25 User's Manual.

char sn_cts(void)Retrieves value of **CTS** pin.**void sn_rts(char b)**Sets the value of **RTS** to *b*.**Completing Serial Communications**

After completing your serial communications, there are a few functions that can be used to reset default system resources.

sn_close**Arguments:** COM *c**Return value:** none

This closes down the serial port, by shutting down the hardware as well as disabling the interrupt.

clean_sern**Arguments:** COM *c**Return value:** none

This flushes the input buffer by resetting the tail and header buffer pointers.

The asynchronous serial I/O ports available on the NEC V25 processor have many other features that might be useful for your application. If you are truly interested in having more control, please read Chapter 11 of the User's Manual for a detailed discussion of other features available to you.

4.4 Functions in SCC.OBJ

The functions found in this object file are prototyped in `scc.h` in the `tern\v25\include` directory.

The SCC is a component that is used to provide a third asynchronous port. It uses the 8 MHz system clock for driving serial communications. The divisors and function arguments for setting up the baud rate for this third port are different than for SER0 and SER1.

| Function Argument | Baud Rate |
|-------------------|----------------|
| 1 | 110 |
| 2 | 150 |
| 3 | 300 |
| 4 | 600 |
| 5 | 1200 |
| 6 | 2400 |
| 7 | 4800 |
| 8 | 9600 (default) |
| 9 | 19,200 |
| 10 | 31,250 |
| 11 | 62,500 |
| 12 | 125,000 |
| 13 | 250,000 |

Unlike the other serial ports, macro service transfer is not used to fill the input buffer for SCC. Instead, an interrupt-service-routine is used to place characters into the input buffer. If the processor does not respond to the interrupt—because it is masked, for example—the interrupt service routine might never be able to complete this process. Over time, this means data might be lost in the SCC as bytes overflow.

Special control registers are used to define how the SCC operates. For a detailed description of registers **MR1** and **MR2**, please see Appendix C of this manual. In most TERN applications, MR1 is set to `0x57`, and MR2 is set to `0x07`. This configures the SCC for no flow control (RTS, CTS not used/checked), no parity, 8-bit, normal operation. Other configurations are also possible, providing self-echo, even-odd parity, up to 2 stop bits, and 5 bit operation, as well as automatic hardware flow control.

Initialization occurs in a manner otherwise similar to SER0 and SER1. A **COM** structure is once again used to hold state information for the serial port. The in-bound and out-bound buffers operate as before, and must be provided upon initialization.

scc_init

Arguments: unsigned char m1, unsigned char m2, unsigned char b, unsigned char* ibuf, int isiz, unsigned char* obuf, int osiz, COM *c

Return value: none

This initializes the SCC2691 serial port to baud rate **b**, as defined in the table above. The values in **m1** and **m2** specify the values to be stored in to **MR1** and **MR2**. As discussed above, these values are normally `0x57` and `0x07`, as shown in TERN sample programs.

ibuf and **isiz** define the input buffer characteristics, and **obuf** and **osiz** define the output buffer.

After initializing the serial port, you must also set up the interrupt service routine. The SCC2691 UART takes up external interrupt **/INT0** on the CPU, and you must set up the appropriate interrupt vector to handle this. An interrupt service routine, **scc_isr()**, has been written to handle the interrupt, and it enables/disables the interrupt as needed to transmit and receive data with the data buffers. So, after initialization, you will need to make a call to do this:

```
int0_init(1, scc_isr);
```

By default, the SCC is disabled for both *transmit* and *receive*. Before using the port, you will need to enable these functionalities.

When using RS232 in full-duplex mode, *transmit* and *receive* functions should both be enabled. Once this is done, you can transmit and receive data as needed. If you do need to do limited flow control, the MPO pin on the J1 header can be used for RTS. For a sample file showing RS232 full duplex communications, please see **ve_scc.c** in the directory **tern\v25\samples\ve**.

RS485 is slightly more complex to use than RS232. RS485 operation is half-duplex only, which means transmission does not occur concurrently with reception. The RS485 driver will echo back bytes sent to the SCC. As a result, assuming you are using the RS485 driver installed on another TERN peripheral board, you will need to disable *receive* while transmitting. While transmitting, you will also need to place the RS485 driver in transmission mode as well. This is done by using **scc_rts(1)**. This uses pin MPO (multi-purpose output), found on the J1 header. While you are receiving data, the RS485 driver will need to be placed in receive mode using **scc_rts(0)**.

en485

Arguments: int i

Return value: none

This function sets the pin MPO either high (i = 1) or low (i = 0). The function **scc_rts()** actually has a similar function, by pulling the same pin high or low, but is intended for use in flow control.

scc_send_e/scc_rec_e

Arguments: none

Return value: none

This function enables transmission or reception on the SCC2691 UART. After initialization, both of these functions are disabled by default. If you are using RS485, only one of these two functions should be enabled at any one time.

scc_send_reset/scc_rec_reset

Arguments: none

Return value: none

This function resets the state of the send and receive function of the SCC2691. One major use of these functions is to disable send and receive. If you are using RS485, you will need to use this feature when transitioning from transmission to reception, or from reception to transmission.

Transmission and reception of data using the SCC is in most ways identical to SER0 and SER1. The functions used to transmit and receive data are similar. For details regarding these functions, please refer to the previous section.

putser_scc

See: **putsern**

putsers_scc

See: **putsersn**

getser_scc
See: `getsern`

getsers_scc
See: `getsersn`

Flow control is also handled in a mostly similar fashion. The CTS pin corresponds to the MPI pin, which is not connected to either of the headers. The RTS pin corresponds to the MPO pin found on the J1 header.

scc_cts
See: `sn_cts`

scc_rts
See: `sn_rts`

Other SCC functions are similar to those for SER0 and SER1.

scc_close
See: `sn_close`

serhit_scc
See: `sn_hit`

clean_ser_scc
See: `clean_sn`

Occasionally, it might also be necessary to check the state of the SCC for information regarding errors that might have occurred. By calling `scc_err`, you can check for framing errors, parity errors (if parity is enabled), and overrun errors.

scc_err
Arguments: none
Return value: unsigned char val

The returned value **val** will be in the form of 0ABC0000 in binary. Bit A is 1 to indicate a framing error. Bit B is 1 to indicate a parity error, and bit C indicates an over-run error.

4.5 Functions in VEEE.OBJ

The 512-byte serial EEPROM (*24C04*) provided on-board provides easy storage of non-volatile program parameters. This is usually an ideal location to store important configuration values that do not need to be changed often. Access to the EEPROM is quite slow, compared to memory access on the rest of the controller.

Part of the EEPROM is reserved for TERN use specifically for this purpose.

Addresses **0x00** to **0x1f** on the EEPROM is reserved for system use, including configuration information about the controller itself, the jump address for Step Two, and other data that is of a more permanent nature.

The rest of the EEPROM memory space, **0x20** to **0x1ff**, is available for your application use.

ee_wr
Arguments: int addr, unsigned char dat
Return value: int status

This function is used to write the passed in **dat** to the specified **addr**. The return value is 0 in success.

ee_rd**Arguments:** int addr**Return value:** int data

This function returns one byte of data from the specified address.

4.6 ADC on C-Engineint **ce_ad12**(unsigned char c);

Operate TLC2543 with P27=/CE, P26=DIN, P25=DOOUT, P24=CLK.

Return the previous ADC result and start a new AD conversion

where: c = input channel

| | |
|--------|-------------------------------|
| c = 0, | input ch = AD0 |
| c = 1, | input ch = AD1 |
| c = 2, | input ch = AD2 |
| c = 3, | input ch = AD3 |
| c = 4, | input ch = AD4 |
| c = 5, | input ch = AD5 |
| c = 6, | input ch = AD6 |
| c = 7, | input ch = AD7 |
| c = 8, | input ch = AD8 |
| c = 9, | input ch = AD9 |
| c = a, | input ch = AD10 |
| c = b, | input ch = (vref+ - vref-) /2 |
| c = c, | input ch = vref- |
| c = d, | input ch = vref+ |
| c = e, | software power down |

returns: 12 bit AD data of the previous conversion !

Unipolar: (Vref+ - Vref-)=0x7ff

Vref- = 0x000

Vref+ = 0xff

Use 1 wait state for Memory and I/O without RDY, < 300 us execution time

Use 0 wait state for Memory and I/O with VEP010, < 270 us execution time

Appendix A: Pin Layout

All dimensions are in inches.

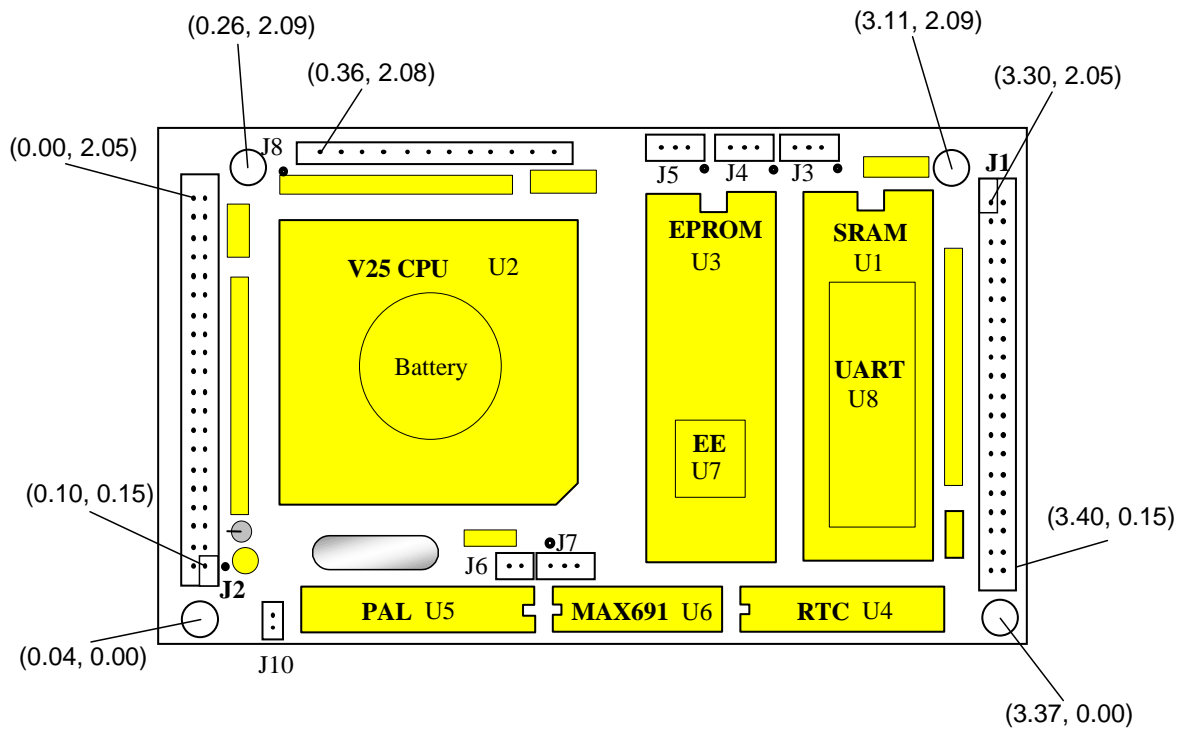


Figure A.1 V-25 Engine Pin Layout

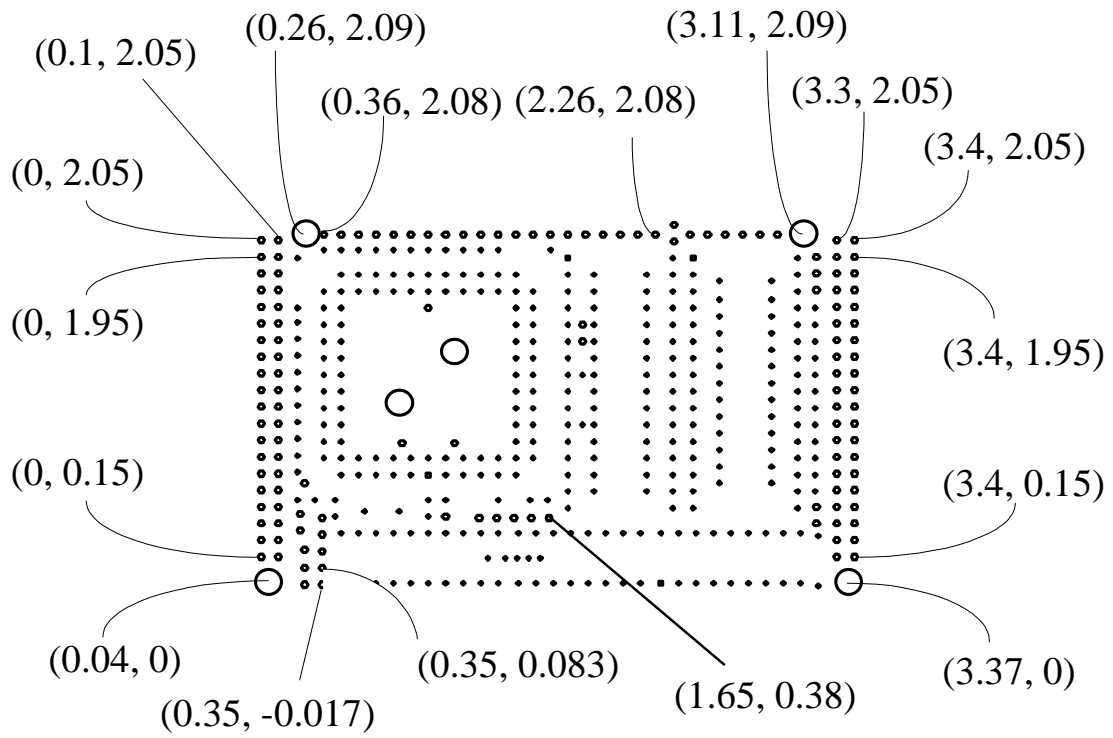
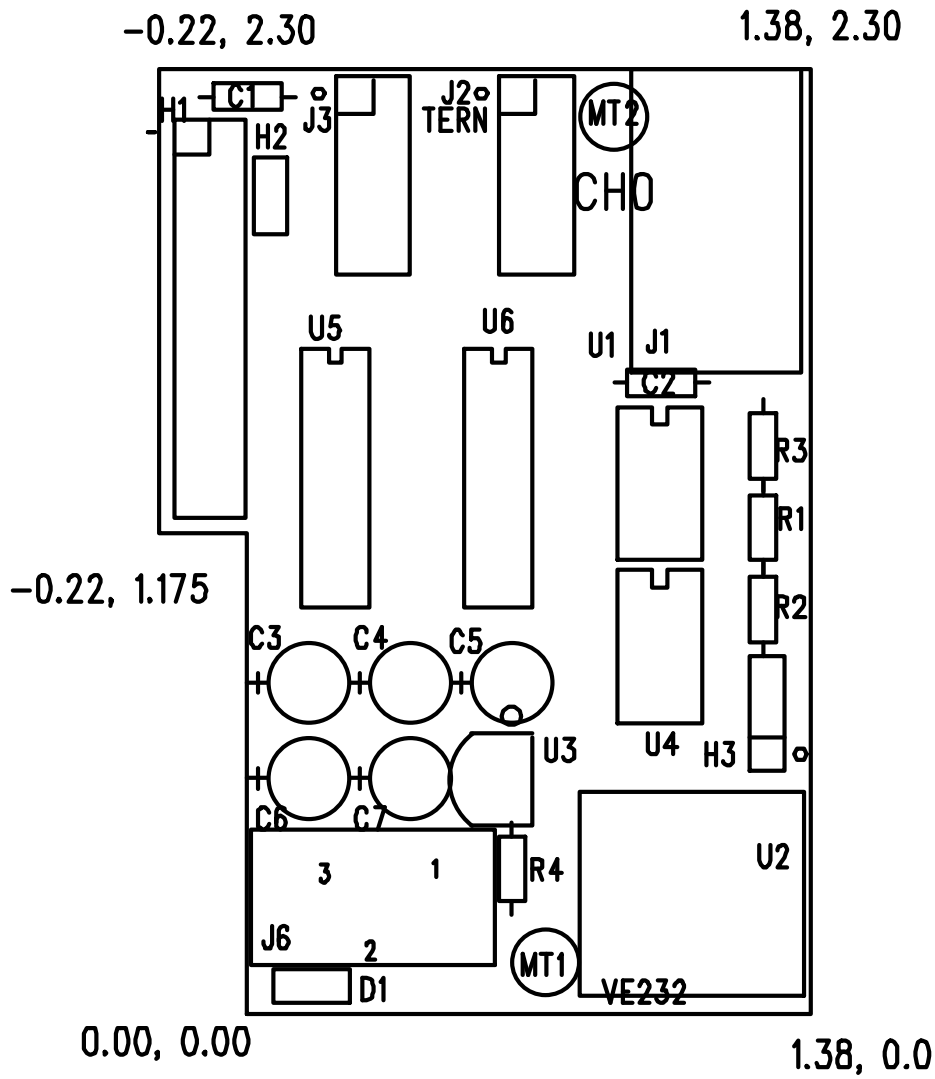


Figure A.2 C-Engine™ Pin Layout

Appendix B: VE232 Pin Layout

All dimensions are in inches.



COMPONENT SIDE

10-21-1994

Appendix C: UART SCC2691

1. Pin Description

| | |
|--------|---|
| D0-D7 | Data bus, active high, bi-directional, and having 3-State |
| /CEN | Chip enable, active-low input |
| /WRN | Write strobe, active-low input |
| /RDN | Read strobe, active-low input |
| A0-A2 | Address input, active-high address input to select the UART registers |
| RESET | Reset, active-high input |
| INTRN | Interrupt request, active-low output |
| X1/CLK | Crystal 1, crystal or external clock input |
| X2 | Crystal 2, the other side of crystal |
| RxD | Receive serial data input |
| TxD | Transmit serial data output |
| MPO | Multi-purpose output |
| MPI | Multi-purpose input |
| Vcc | Power supply, +5 V input |
| GND | Ground |

2. Register Addressing

| A2 | A1 | A0 | READ (RDN=0) | WRITE (WRN=0) |
|----|----|----|--------------|---------------|
| 0 | 0 | 0 | MR1,MR2 | MR1, MR2 |
| 0 | 0 | 1 | SR | CSR |
| 0 | 1 | 0 | BRG Test | CR |
| 0 | 1 | 1 | RHR | THR |
| 1 | 0 | 0 | 1x/16x Test | ACR |
| 1 | 0 | 1 | ISR | IMR |
| 1 | 1 | 0 | CTU | CTUR |
| 1 | 1 | 1 | CTL | CTLR |

Note:

- ACR = Auxiliary control register
- BRG = Baud rate generator
- CR = Command register
- CSR = Clock select register
- CTL = Counter/timer lower
- CTLR = Counter/timer lower register
- CTU = Counter/timer upper
- CTUR = Counter/timer upper register
- MR = Mode register
- SR = Status register
- RHR = Rx holding register
- THR = Tx holding register

3. Register Bit Formats

MR1 (Mode Register 1):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|-------------------|-----------------------|--|-------|---|--------------------------------------|-------|
| RxRTS | RxINT | Error | ___Parity Mode___ | | Parity Type | Bits per Character | |
| 0 = no 1 = yes | 0=RxDY 1=FFULL | 0 = char 1 = block | 00 = with parity 01 = Force parity 10 = No parity 11 = Special mode | | 0 = Even 1 = Odd In Special mode: 0 = Data 1 = Addr | 00 = 5 01 = 6 10 = 7 11 = 8 | |

MR2 (Mode Register 2):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------|-------------------|-------------------|--|--|--|--|
| Channel Mode | | TxRTS | CTS Enable Tx | Stop Bit Length (add 0.5 to cases 0-7 if channel is 5 bits/character) | | | |
| 00 = Normal 01 = Auto echo 10 = Local loop 11 = Remote loop | | 0 = no 1 = yes | 0 = no 1 = yes | 0 = 0.563 1 = 0.625 2 = 0.688 3 = 0.750 | 4 = 0.813 5 = 0.875 6 = 0.938 7 = 1.000 | 8 = 1.563 9 = 1.625 A = 1.688 B = 1.750 | C = 1.813 D = 1.875 E = 1.938 F = 2.000 |

CSR (Clock Select Register):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|-------|-------|-------|--|-------|-------|-------|
| Receiver Clock Select | | | | Transmitter Clock Select | | | |
| when ACR[7] = 0: 0 = 50 1 = 110 2 = 134.5 3 = 200 4 = 300 5 = 600 6 = 1200 7 = 1050 8 = 2400 9 = 4800 A = 7200 B = 9600 C = 38.4k D = Timer E = MPI-16x F = MPI-1x when ACR[7] = 1: 0 = 75 1 = 110 2 = 134.5 3 = 150 4 = 300 5 = 600 6 = 1200 7 = 2000 8 = 2400 9 = 4800 A = 7200 B = 1800 C = 19.2k D = Timer E = MPI-16x F = MPI-1x | | | | when ACR[7] = 0: 0 = 50 1 = 110 2 = 134.5 3 = 200 4 = 300 5 = 600 6 = 1200 7 = 1050 8 = 2400 9 = 4800 A = 7200 B = 9600 C = 38.4k D = Timer E = MPI-16x F = MPI-1x when ACR[7] = 1: 0 = 75 1 = 110 2 = 134.5 3 = 150 4 = 300 5 = 600 6 = 1200 7 = 2000 8 = 2400 9 = 4800 A = 7200 B = 1800 C = 19.2k D = Timer E = MPI-16x F = MPI-1x | | | |

CR (Command Register):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|-----------------|------------------------|------------------|---------------|--------------|---------------|--------------|
| Miscellaneous Commands | | | | Disable Tx | Enable Tx | Disable Rx | Enable Rx |
| 0 = no command | 8 = start C/T | 1 = reset MR pointer | 9 = stop counter | 0 = no | 0 = no | 0 = no | 0 = no |
| 2 = reset receiver | A = assert RTSN | 3 = reset transmitter | B = negate RTSN | 1 = yes | 1 = yes | 1 = yes | 1 = yes |
| 4 = reset error status | C = reset MPI | 5 = reset break change | change INT | | | | |
| | D = reserved | INT | D = reserved | | | | |
| 6 = start break | E = reserved | 7 = stop break | F = reserved | | | | |

SR (Channel Status Register):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------------------------|------------------------|------------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Received Break | Framing Error | Parity Error | Overrun Error | TxE _{MT} | TxR _{DY} | FFULL | RxR _{DY} |
| 0 = no 1 = yes * | 0 = no 1 = yes * | 0 = no 1 = yes * | 0 = no 1 = yes | 0 = no 1 = yes | 0 = no 1 = yes | 0 = no 1 = yes | 0 = no 1 = yes |

Note:

* These status bits are appended to the corresponding data character in the receive FIFO. A read of the status register provides these bits [7:5] from the top of the FIFO together with bits [4:0]. These bits are cleared by a reset error status command. In character mode they are reset when the corresponding data character is read from the FIFO.

ACR (Auxiliary Control Register):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--|---|-------|-------|---|--|-------|-------|
| BRG Set Select | Counter/Timer Mode and Source | | | Power-Down Mode | MPO Pin Function Select | | |
| 0 = Baud rate set 1, see CSR bit format 1 = Baud rate set 2, see CSR bit format | 0 = counter, MPI pin 1 = counter, MPI pin divided by 16 2 = counter, TxC-1x clock of the transmitter 3 = counter, crystal or external clock (x1/CLK) 4 = timer, MPI pin 5 = timer, MPI pin divided by 16 6 = timer, crystal or external clock (x1/CLK) 7 = timer, crystal or external clock (x1/CLK) divided by 16 | | | 0 = on, power down active 1 = off normal | 0 = RTSN 1 = C/TO 2 = TxC (1x) 3 = TxC (16x) 4 = RxC (1x) 5 = RxC (16x) 6 = TxRDY 7 = RxRDY/FFULL | | |

ISR (Interrupt Status Register):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------------------|-----------------------|----------|-------------------|-------------------|-------------------|-------------------|-------------------|
| MPI Pin Change | MPI Pin Current State | Not Used | Counter Ready | Delta Break | RxRDY/FFULL | TxEINT | TxRDY |
| 0 = no 1 = yes | 0 = low 1 = high | | 0 = no 1 = yes | 0 = no 1 = yes | 0 = no 1 = yes | 0 = no 1 = yes | 0 = no 1 = yes |

IMR (Interrupt Mask Register):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------------------|---------------------|----------|-------------------------|-----------------------|-----------------------|-------------------|-------------------|
| MPI Change Interrupt | MPI Level Interrupt | Not Used | Counter Ready Interrupt | Delta Break Interrupt | RxRDY/FFULL Interrupt | TxEINT Interrupt | TxRDY Interrupt |
| 0 = off 1 = 0n | 0 = off 1 = 0n | | 0 = off 1 = 0n | 0 = off 1 = 0n | 0 = off 1 = 0n | 0 = off 1 = 0n | 0 = off 1 = 0n |

CTUR (Counter/Timer Upper Register):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|----------|----------|----------|----------|----------|----------|---------|---------|
| C/T [15] | C/T [14] | C/T [13] | C/T [12] | C/T [11] | C/T [10] | C/T [9] | C/T [8] |

CTLR (Counter/Timer Lower Register):

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| C/T [7] | C/T [6] | C/T [5] | C/T [4] | C/T [3] | C/T [2] | C/T [1] | C/T [0] |

Appendix D: RTC72421 / 72423

Function Table

| Address | | | | Data | | | | Count Value | Remarks | |
|----------------|----------------|----------------|----------------|------------------|-----------------|------------------|------------------|------------------|------------------|-------------------------------|
| A ₃ | A ₂ | A ₁ | A ₀ | Register | D ₃ | D ₂ | D ₁ | | | D ₀ |
| 0 | 0 | 0 | 0 | S ₁ | s ₈ | s ₄ | s ₂ | s ₁ | 0~9 | 1-second digit register |
| 0 | 0 | 0 | 1 | S ₁₀ | | s ₄₀ | s ₂₀ | s ₁₀ | 0~5 | 10-second digit register |
| 0 | 0 | 1 | 0 | MI ₁ | mi ₈ | mi ₄ | mi ₂ | mi ₁ | 0~9 | 1-minute digit register |
| 0 | 0 | 1 | 1 | MI ₁₀ | | mi ₄₀ | mi ₂₀ | mi ₁₀ | 0~5 | 10-minute digit register |
| 0 | 1 | 0 | 0 | H ₁ | h ₈ | h ₄ | h ₂ | h ₁ | 0~9 | 1-hour digit register |
| 0 | 1 | 0 | 1 | H ₁₀ | | PM/AM | h ₂₀ | h ₁₀ | 0~2 or 0~1 | PM/AM, 10-hour digit register |
| 0 | 1 | 1 | 0 | D ₁ | d ₈ | d ₄ | d ₂ | d ₁ | 0~9 | 1-day digit register |
| 0 | 1 | 1 | 1 | D ₁₀ | | | d ₂₀ | d ₁₀ | 0~3 | 10-day digit register |
| 1 | 0 | 0 | 0 | MO ₁ | mo ₈ | mo ₄ | mo ₂ | mo ₁ | 0~9 | 1-month digit register |
| 1 | 0 | 0 | 1 | MO ₁₀ | | | | mo ₁₀ | 0~1 | 10-month digit register |
| 1 | 0 | 1 | 0 | Y ₁ | y ₈ | y ₄ | y ₂ | y ₁ | 0~9 | 1-year digit register |
| 1 | 0 | 1 | 1 | Y ₁₀ | y ₈₀ | y ₄₀ | y ₂₀ | y ₁₀ | 0~9 | 10-year digit register |
| 1 | 1 | 0 | 0 | W | | w ₄ | w ₂ | w ₁ | 0~6 | Week register |
| 1 | 1 | 0 | 1 | Reg D | 30s Adj | IRQ Flag | Busy | Hold | | Control register D |
| 1 | 1 | 1 | 0 | Reg E | t ₁ | t ₀ | INT/ STD | Mask | | Control register E |
| 1 | 1 | 1 | 1 | Reg F | Test | 24/ 12 | Stop | Rest | | Control register F |

Note: 1) INT/STD = Interrupt/Standard, Rest = Reset;

2) Mask AM/PM bit with 10's of hours operations;

3) Busy is read only, IRQ can only be set low ("0");

4)

| Data bit | PM/AM | INT/STD | 24/12 |
|----------|-------|---------|-------|
| 1 | PM | INT | 24 |
| 0 | AM | STD | 12 |

5) Test bit should be "0".

Appendix E: Serial EEPROM Map

Part of the on-board serial EEPROM locations are used by system software. Application programs must not use these locations.

| | |
|------|-------------------------------|
| 0x00 | Node Address, for networking |
| 0x01 | Board Type |
| | 00 VE |
| | 10 CE |
| | 01 BB |
| | 02 PD |
| | 03 SW |
| | 04 TD |
| | 05 MC |
| 0x02 | |
| 0x03 | |
| 0x04 | SER0_receive, used by ser0.c |
| 0x05 | SER0_transmit, used by ser0.c |
| 0x06 | SER1_receive, used by ser1.c |
| 0x07 | SER1_transmit, used by ser1.c |
| 0x10 | CS high byte, used by ACTR™ |
| 0x11 | CS low byte, used by ACTR™ |
| 0x12 | IP high byte, used by ACTR™ |
| 0x13 | IP low byte, used by ACTR™ |
| 0x18 | MM page register 0 |
| 0x19 | MM page register 1 |
| 0x1a | MM page register 2 |
| 0x1b | MM page register 3 |

Appendix F: Software Glossary

The following is a glossary of library functions for the V25-Engine.

void ve_init(void) ve.h

Initializes the V25 processor. The following is the source code for *ve_init()*

```
pokeb(0xffff,0x02,0x80); /* Set PMC0 P07=CLK */
pokeb(0xffff,0x01,0xd7); /* Set PM0 for input, P05=LED P03=HWD output */
pokeb(0xffff,0x0a,0x80); /* Set PMC1 P17 for READY */
pokeb(0xffff,0x09,0xaf); /* Set PM1 for input, P14=RTS1,P16=RTS0 OUTPUT */
pokeb(0xffff,0x12,0x00); /* Set P20-P27 for port mode */
pokeb(0xffff,0x11,0xf7); // Set PM2 for input, P23=EN485 output
```

Reference: led.c

void ve_reset(void) ve.h

Resets the V25 processor.

void delay_ms(int m) ve.h

Approximate microsecond delay. Does not use timer.

Var: m - Delay in approximate ms

Reference: led.c

void led(int i) ve.h

Toggles P05 used for led.

Var: i - Led on or off

Reference: led.c

void delay0(unsigned int t) ve.h

Approximate loop delay. Does not use timer.

Var: m - Delay using simple for loop up to t.

Reference:

void halt(void)

ve.h

Enables HALT standby mode, which halts the system clock to reduce power consumption. Peripheral CPU devices (serial ports, timers, DMA) will not be effected. System clock restored by interrupt.

Reference: `ve_halt.c`

void hitwd(void)

ve.h

Hits the watchdog timer using P03. P03 must be connected to WDI of the MAX691 supervisor chip.

Reference: *See the Hardware chapter of this manual for more information on the MAX691.*

void port_init(char p, char pmc, char pm)

ve.h

Initializes I/O port mode control and port mode.

Var: `p` = port 0, 1 or 2.

The *PMC* and *PM* variables define each pin of the 8-bit port selected.

For example: *PM* = `0xf0` would set bits 0 – 3 as low and bits 4 – 7 as high.

`pmc` = CONTROL or I/O mode (0 = I/O; 1 = CONTROL).

`pm` = I/O pin as input or output(0 = output; 1 = input).

Reference: `portx.c`

void port_wr(char p, char dat)

ve.h

Writes a bit to a Port I/O line. Port I/O line must be in an output mode

Var: `p` - Port 0, 1, or 2

`dat` - 8-bit data for port `p`

Reference: `portx.c`

unsigned int port_rd(char p)

ve.h

Reads an 8-bit I/O port.

Var: `port` - 0: Port 0

1: Port 1

2: Port 2

Reference: `portx.c`

void portt_wr(char vref)

ve.h

Selects reference voltage for the comparator input port.

Var: vref - {0 ... 15} defines reference as follows
 $reference = V_{th} * vref / 16.$
 For vref - 0: $reference = V_{th}.$
 Vth : Threshold voltage $\approx 3.57V$

Reference: portt.c

char portt_rd(void)

ve.h

Reads from the 8-bit comparator input port. Returns 8-bit value.

bit = 0, $PT_n < V_{ref}$

bit = 1, $PT_n > V_{ref}$

where PT_n is the input voltage and V_{ref} is the selected threshold voltage.

Reference: portt.c

void outport(int portid, int value)

dos.h

Writes 16-bit *value* to I/O address *portid*.

Var: portid - I/O address
 value - 16 bit value

void outportb(int portid, int value)

dos.h

Writes 8-bit *value* to I/O address *portid*.

Var: portid - I/O address
 value - 8 bit value

int inport(int portid)

dos.h

Reads from an I/O address *portid*. Returns 16-bit value.

Var: portid - I/O address

int inportb(int portid)

dos.h

Reads from an I/O address *portid*. Returns 8-bit value.

Var: portid - I/O address

int ee_wr(int addr, unsigned char dat) veee.h

Writes to the serial EEPROM.

Var: addr - EEPROM data address
 dat - data

Reference: *ve_ee.c*

int ee_rd(int addr) veee.h

Reads from the serial EEPROM. Returns 8-bit data

Var: addr - EEPROM data address

Reference: *ve_ee.c*

*void rtc_init(unsigned char * time)* ve.h

Sets real time clock date, year and time.

Var: time - time and date string
 String sequence is the following:
 time[0] = weekday
 time[1] = year10
 time[2] = year1
 time[3] = mon10
 time[4] = mon1
 time[5] = day10
 time[6] = day1
 time[7] = hour10
 time[8] = hour1
 time[9] = min10
 time[10] = min1
 time[11] = sec10
 time[12] = sec1
 unsigned char time[]={2,9,8,0,7,0,1,1,3,1,0,2,0};
 /* Tuesday, July 01, 1998, 13:10:20 */

Reference: *rtc_init.c*

*int rtc_rd(TIM *r)* ve.h

Reads from the real-time clock.

Var: *r - Struct type TIM for all of the RTC data
 typedef struct{
 unsigned char sec1, sec10, min1, min10, hour1, hour10;
 unsigned char day1, day10, mon1, mon10, year1, year10;
 unsigned char wk;
 } TIM;

Reference: *rtc.c*

void timer0_init(unsigned char mode, int md0, int tm0); ve.h

| b | Baud |
|----|------------------|
| 6 | 2400 |
| 7 | 4800 |
| 8 | 9600 |
| 9 | 19,200 (default) |
| 10 | 38,400 |
| 11 | 57,600 |
| 12 | 76,800 |
| 13 | 115,000 |
| 14 | 230,000 |
| 15 | 460,800 |
| 16 | 1 Meg |

Reference: s0_echo.c, s1_echo.c, s1_0.c

void scc_init(unsigned char m1, unsigned char m2, unsigned char b, unsigned char* ibuf, int isiz, unsigned char* obuf, int osiz, COM *c) scc.h

Serial port 0, 1 initialization.

Var: m1 = SCC691 MR1
 m2 = SCC691 MR2
 b - baud rate.
 ibuf - pointer to input buffer array
 isiz - input buffer size
 obuf - pointer to output buffer array
 osiz - output buffer size
 c - pointer to serial port structure. See VE.H for COM structure.

| m1 bit | Definition |
|--------|---|
| 7 | (RxRTS) receiver request-to-send control, 0=no, 1=yes |
| 6 | (RxINT) receiver interrupt select, 0=RxRDY, 1=FIFO FULL |
| 5 | (Error Mode) Error Mode Select, 0 = Char., 1=Block |
| 4-3 | (Parity Mode), 00=with, 01=Force, 10=No, 11=Special |
| 2 | (Parity Type), 0=Even, 1=Odd |
| 1-0 | (# bits) 00=5, 01=6, 10=7, 11=8 |

| m2 bit | Definition |
|--------|---|
| 7-6 | (Modes) 00=Normal, 01=Echo, 10=Local loop, 11=Remote loop |
| 5 | (TxRTS) Transmit RTS control, 0=No, 1= Yes |
| 4 | (CTS Enable Tx), 0=No, 1=Yes |
| 3-0 | (Stop bit), 0111=1, 1111=2 |

| b | baud |
|----|--------|
| 1 | 110 |
| 2 | 150 |
| 3 | 300 |
| 4 | 600 |
| 5 | 1200 |
| 6 | 2400 |
| 7 | 4800 |
| 8 | 9600 |
| 9 | 19200 |
| 10 | 31250 |
| 11 | 62500 |
| 12 | 125000 |
| 13 | 250000 |

Reference: `s0_echo.c`, `s1_echo.c`, `s1_0.c`

| | |
|--|--------|
| <i>int putser0(unsigned char ch, COM *c);</i> | ser0.h |
| <i>int putser1(unsigned char ch, COM *c);</i> | ser1.h |
| <i>int putser_scc(unsigned char ch, COM *c);</i> | scc.h |

Output 1 character to serial port. Character will be sent to serial output with interrupt isr.

Var: `ch` - character to output
`c` - pointer to serial port structure

Reference: `s0_echo.c`, `s1_echo.c`, `s1_0.c`

| | |
|---|--------|
| <i>int putsers0(unsigned char *str, COM *c);</i> | ser0.h |
| <i>int putsers1(unsigned char *str, COM *c);</i> | ser1.h |
| <i>int putsers_scc(unsigned char ch, COM *c);</i> | scc.h |

Outputs a character string to serial port. Character will be sent to serial output with interrupt isr.

Var: `str` - pointer to output character string
`c` - pointer to serial port structure

Reference: `ser1_sin.c`

| | |
|--------------------------------|--------|
| <i>int serhit0(COM *c);</i> | ser0.h |
| <i>int serhit1(COM *c);</i> | ser1.h |
| <i>int serhit_scc(COM *c);</i> | scc.h |

Checks input buffer for new input characters. Returns 1 if new character is in input buffer, else 0.

Var: `c` - pointer to serial port structure

Reference: `s0_echo.c`, `s1_echo.c`, `s1_0.c`

| | |
|--|--------|
| <i>unsigned char getser0(COM *c);</i> | ser0.h |
| <i>unsigned char getser1(COM *c);</i> | ser1.h |
| <i>unsigned char getser_scc(COM *c);</i> | scc.h |

Retrieves 1 character from the input buffer. Assumes that *serhit* routine was evaluated.

Var: `c` - pointer to serial port structure

Reference: `s0_echo.c`, `s1_echo.c`, `s1_0.c`

| | |
|--|--------|
| <i>int getsers0(COM *c, int len, unsigned char *str);</i> | ser0.h |
| <i>int getsers1(COM *c, int len, unsigned char *str);</i> | ser1.h |
| <i>int getsers_scc(COM *c, int len, unsigned char *str);</i> | scc.h |

Retrieves a fixed-length character string from the input buffer. If the buffer contains less characters than the length requested, *str* will contain only the remaining characters from the buffer. Appends a '\0' character to the end of *str*. Returns the retrieved string length.

Var: `c` - pointer to serial port structure
`len` - desired string length
`str` - pointer to output character string

Reference: `ser1.h`, `ser0.h` for source code.

G-1 Functional Description

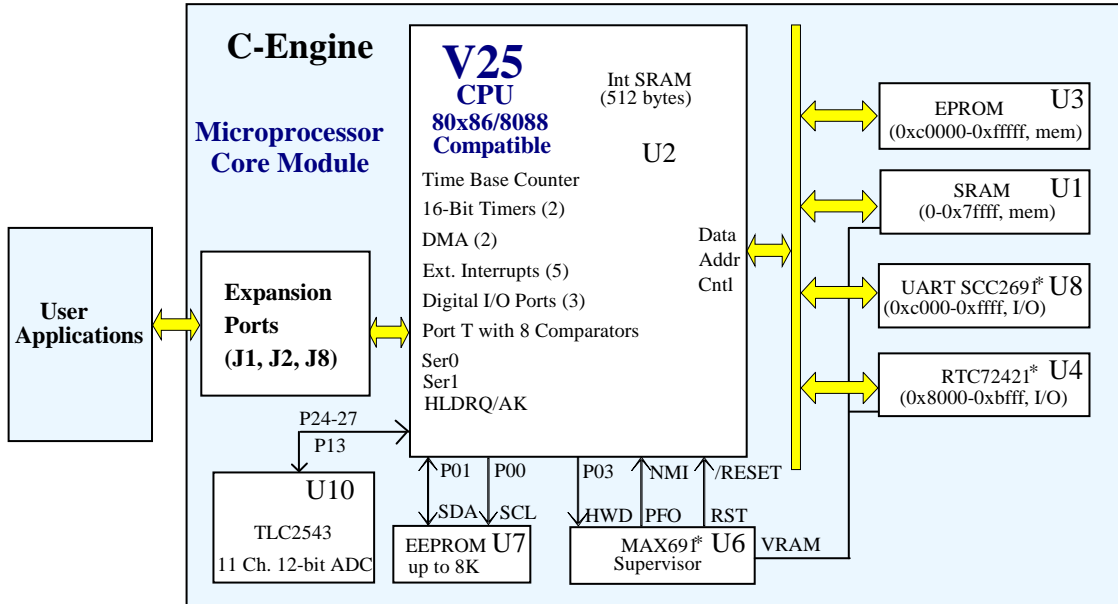


Fig. G.1 Functional block diagram of the C-Engine™

G-2 Physical Description

The physical layout of the C-Engine™ is shown in Fig. 1.2. The components with dashed line shown in Fig. 1.2 are located underneath other chips. The small circles denote the PIN 1 positions.

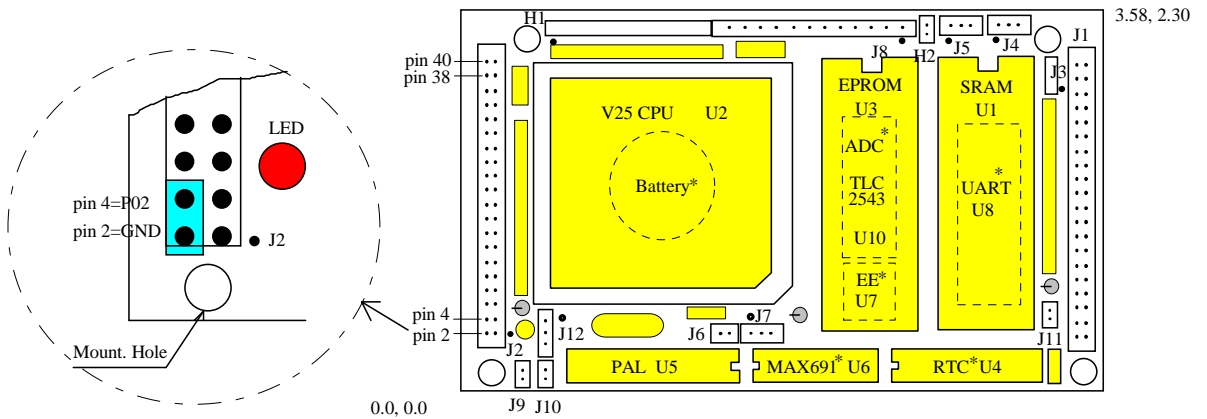


Fig. G.2 Physical layout of C-Engine™The components with "*" are optional.

G-3 I/O lines available

Some I/O lines are used by the C-Engine™ system as listed below:
 P00 I/O EEPROM (U7 pin 6) clock SCL

| | | |
|------|-----------|---|
| P01 | I/O | EEPROM (U7 pin 5) data SDA |
| P02 | I/O | J2 pin 4. If low, jump to application code which starting address is defined in the on board EEPROM (0x10 to 0x13). |
| P03* | I/O | J6 pin2. HWD (Hit watchdog) |
| P04* | I/O | WDO (Read watchdog output, U6 pin 14). |
| P05* | I/O | J2 pin 5, on board LED control |
| P06 | I/O | J2 pin 3. |
| P07 | clock out | J1 pin 4, CLKOUT, 8 MHz as system clock. |
| P10 | NMI | J10 pin 2, PFO (Power Failure Output), if J10 jumper is on. |
| P11* | INTP0 | J2 pin 8, External Interrupt Input0, falling edge effective. C-Engine™ U8 SCC2691 UART interrupt. |
| P12 | INTP1 | J2 pin 6, External Interrupt Input1, falling edge effective. |
| P13 | INTP2 | J2 pin 33, External Interrupt Input2, falling edge effective. |
| P14* | I/O | J2 pin 31, may be used as RTS1 for SER1. |
| P15 | I/O | J2 pin 29. |
| P16* | I/O | J2 pin 27, may be used as RTS0 for SER0. |
| P17 | RDY | J1 pin 27, V25 ready signal, used for more wait states. |
| P20 | I/O(DR0) | J2 pin 30, counter 0/DMA channel 0 request, rising edge active. |
| P21 | I/O(DA0) | J9 pin 1, DMA channel 0 Ack, active low, if J9 jumper on. |
| P22 | I/O | J2 pin 38. |
| P23 | I/O | J2 pin 24, counter 1/DMA1/EN485 for SCC RS485 driver. |
| P24 | I/O | J2 pin 20 and ADC SCLK. |
| P25 | I/O | J2 pin 18 and ADC DIN. |
| P26 | I/O | J2 pin 14 and ADC DOUT. |
| P27 | I/O | J2 pin 12 and ADC /CS. |
| PT0 | INPUT | J2 pin 23. |
| PT1 | INPUT | J2 pin 21. |
| PT2 | INPUT | J2 pin 19. |
| PT3 | INPUT | J2 pin 17. |
| PT4 | INPUT | J2 pin 15. |
| PT5 | INPUT | J2 pin 13. |
| PT6 | INPUT | J2 pin 11. |
| PT7* | INPUT | J1 pin 11, PFI (Power Failure Input, if PFI<1.3V, reset) |

G-4 Jumper Settings

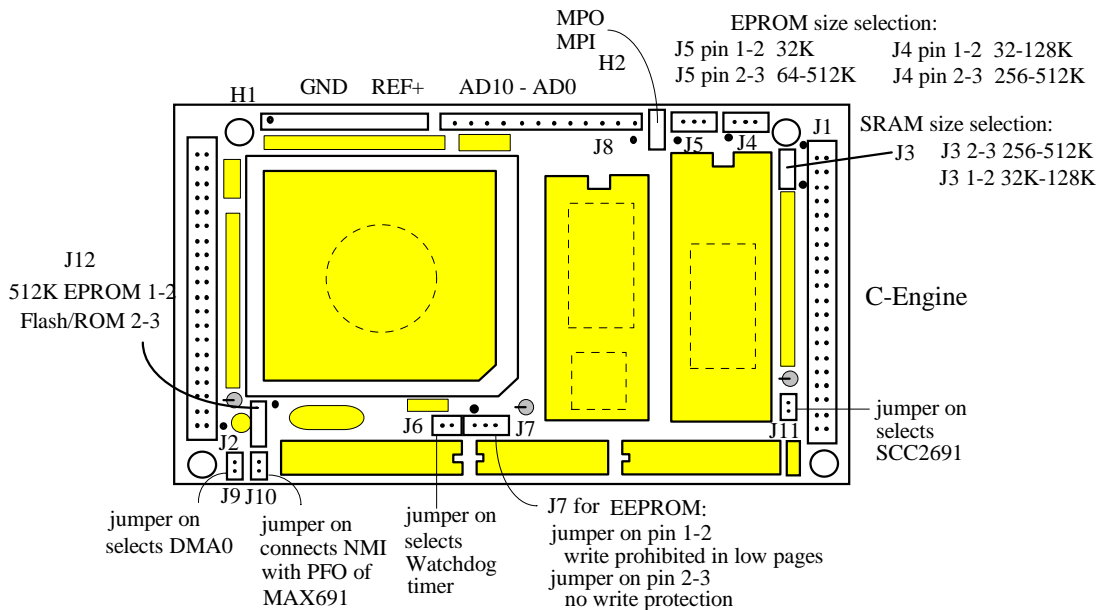


Fig. G.3 Jumper settings on C-Engine™

G-5 12-bit ADC (TLC2543)

The TLC2543 is a 12-bit, switched-capacitor, successive-approximation, 11 channels, serial interface, analog-to-digital converter. It has three control inputs (/CS=P27; CLK=P24; DIN=P25) and is designed for communication with a host through a serial tri-state output (DOUT=P26). If P27 is low, the TLC2543 will have output on P26. If P27 is high, the TLC2543 is disabled and P24, P25, P26 are free. P27 is pulled high by a 10K resistor on board. The TLC2543 has an on-chip 14 channel multiplexer that can select any one of 11 inputs or any one of three internal self-test voltages. The sample-and-hold function is automatic. At the end of conversion, the end-of-conversion (EOC=P13) output goes high to indicate that conversion is complete. TLC2543 features differential high-impedance inputs that facilitate ratiometric conversion, scaling, and isolation of analog circuitry from logic and supply noise. A switched-capacitor design allows low-error conversion over the full operating temperature range. The analog input signal source impedance should be less than 50Ω and capable of slewing the analog input voltage into a 60 pF capacitor.

In order to operate the TLC2543, 5 V25 I/O lines are used as listed below:

| | |
|------|--|
| /CS | Chip select = P27, high to low transition enables DOUT, DIN and CLK. low to high transition disables DOUT, DIN and CLK. |
| DIN | P25, serial data input |
| DOUT | P26, 3-state serial data output. |
| EOC | P13, End of Conversion, high indicates conversion complete and data is ready |
| CLK | I/O clock = P24 |
| REF+ | Upper reference voltage (normally VCC) |
| REF- | Lower reference voltage (normally GND) |
| VCC | Power supply, +5 V input |
| GND | Ground |

The analog inputs AD0 to AD10 are available at J8 connector. REF+, GND, VCC are available at H1.

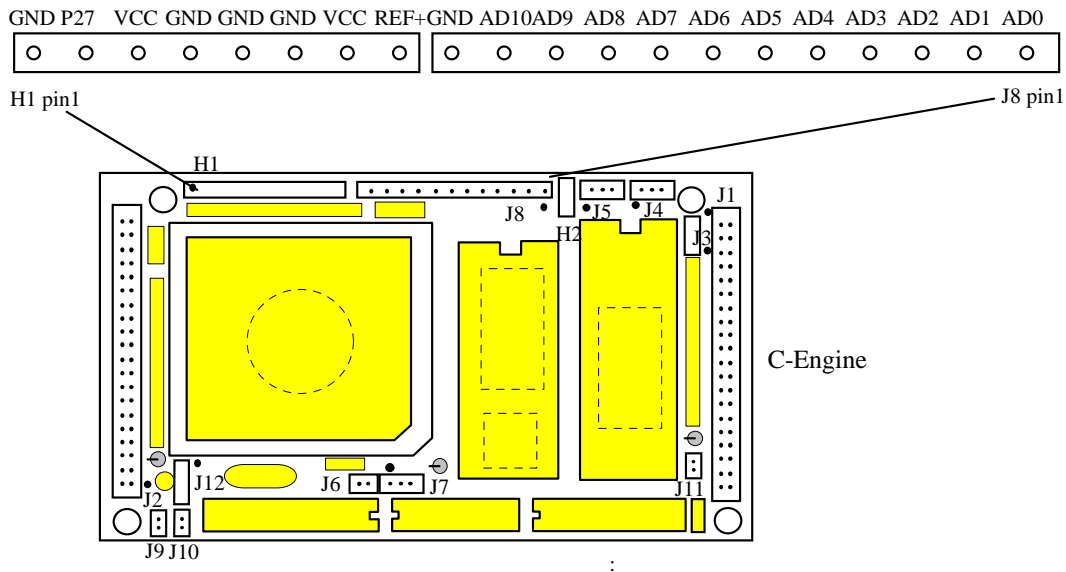


Fig. 1.4 H1 and J8

1-6 Jumpers and Headers

There are 14 jumpers and connectors on the C-Engine™.

| Name | Size | Function |
|------|------|--|
| J1 | 20x2 | main expansion port |
| J2 | 20x2 | main expansion port |
| J3 | 3x1 | SRAM selection: pin 2-3 SRAM 256K-512K, pin 1-2 SRAM 32K-128K |
| J4 | 3x1 | EPROM size selection: pin 1-2 EPROM size 32K-128K pin 2-3 EPROM size 256K-512K |
| J5 | 3x1 | EPROM size selection: pin 1-2 EPROM size 32K pin 2-3 EPROM size 64K-512K |
| J6 | 2x1 | Watchdog timer is enabled, if Jumper is on. Disabled, if jumper is off |
| J7 | 3x1 | pin 1-2 EEPROM write prohibited in low pages pin 2-3 No EEPROM write protection |
| J8 | 12x1 | AD0-10, 11 channels of analog inputs. |
| J9 | 2x1 | pin 1=P21, pin2=/DA0, DMA channel 0 is selected, if a jumper is on DMA0 is not selected, if no jumper, P21,P20=/DR0 can be used as I/O pins |
| J10 | 2x1 | pin 1=/PFO, pin2=/NMI. If jumper is on, when power failure is sensed, PFO of MAX691 will generate an NMI interrupt |
| J11 | 2x1 | A jumper must put on this connector in order to select SCC2691 UART. |
| J12 | 3x1 | 512K EPROM pin 1-2; 32K-256K EPROM/EEPROM pin 2-3 |
| H1 | 8x1 | REF+, VCC, GND, P27(LTC2543 ADC CS) |
| H2 | 2x1 | UART SCC2691 MPO and MPI |
| J15 | 2x1 | pin 1= REF+, pin 2 = VCC. J15 is located next to TLC2543 pin 14 and pin 15. |

A wire jumper may be soldered on the back side (solder side) of the C-Engine™ connecting REF+=VCC. If you want to provide your reference voltage for the ADC, you need to cut off that wire and provide your reference from J8 connector.

G-7 Software: ADC

int **ce_ad12**(unsigned char c);

Operate TLC2543 with P27=/CE, P26=DIN, P25=DOOUT, P24=CLK.

Return the previous ADC result and start a new AD conversion

where: c = input channel

c = 0, input ch = AD0
 c = 1, input ch = AD1
 c = 2, input ch = AD2
 c = 3, input ch = AD3
 c = 4, input ch = AD4
 c = 5, input ch = AD5
 c = 6, input ch = AD6
 c = 7, input ch = AD7
 c = 8, input ch = AD8
 c = 9, input ch = AD9
 c = a, input ch = AD10
 c = b, input ch = (vref+ - vref-) / 2
 c = c, input ch = vref-
 c = d, input ch = vref+
 c = e, software power down

returns: 12 bit AD data of the previous conversion !

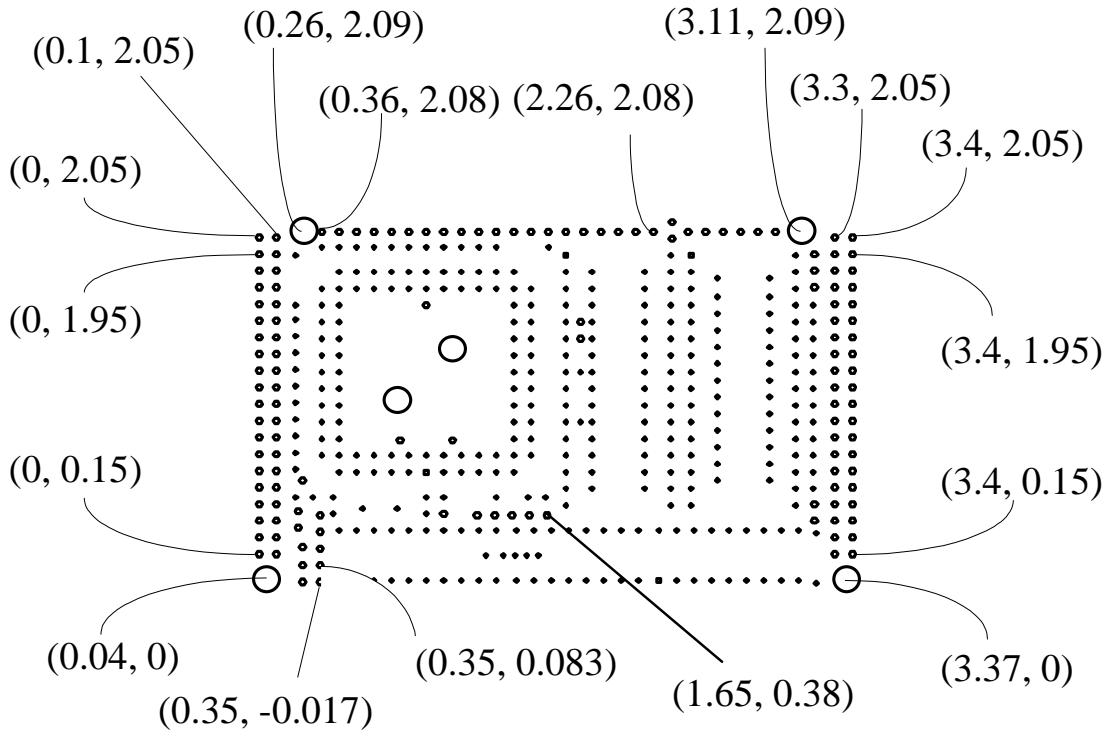
Unipolar: (Vref+ - Vref-)=0x7ff
 Vref- = 0x000
 Vref+ = 0xfff

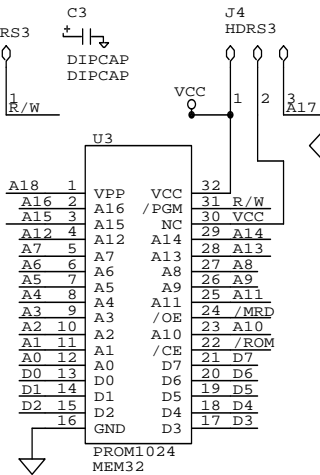
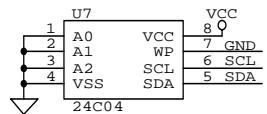
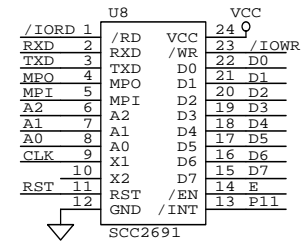
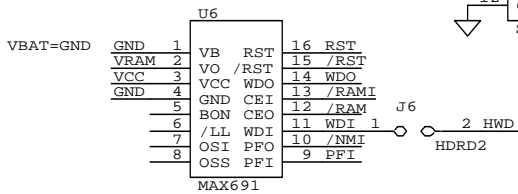
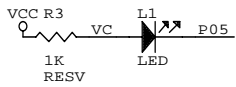
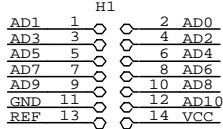
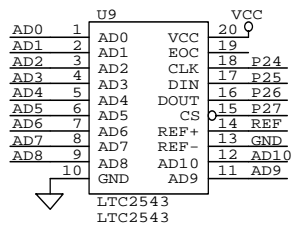
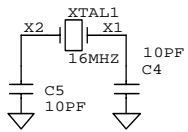
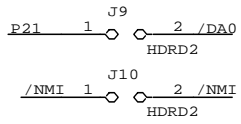
Use 1 wait state for Memory and I/O without RDY, < 300 us execution time

Use 0 wait state for Memory and I/O with VEP010, < 270 us execution time

G-8 Pin Layout of the C-Engine™

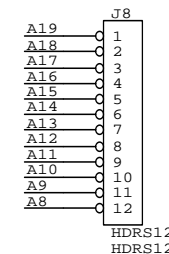
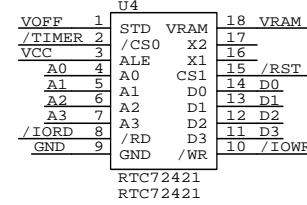
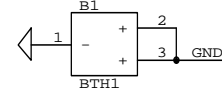
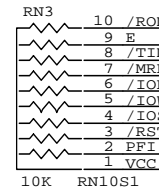
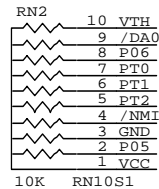
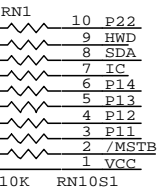
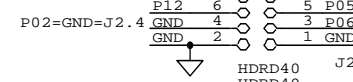
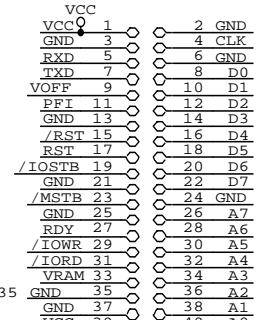
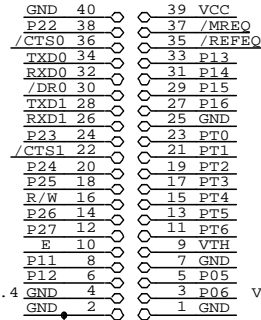
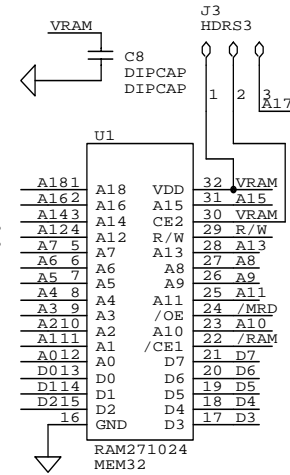
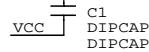
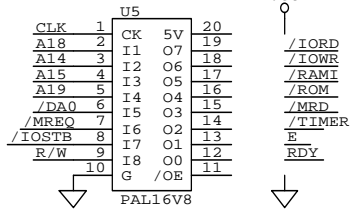
All dimensions are in inches



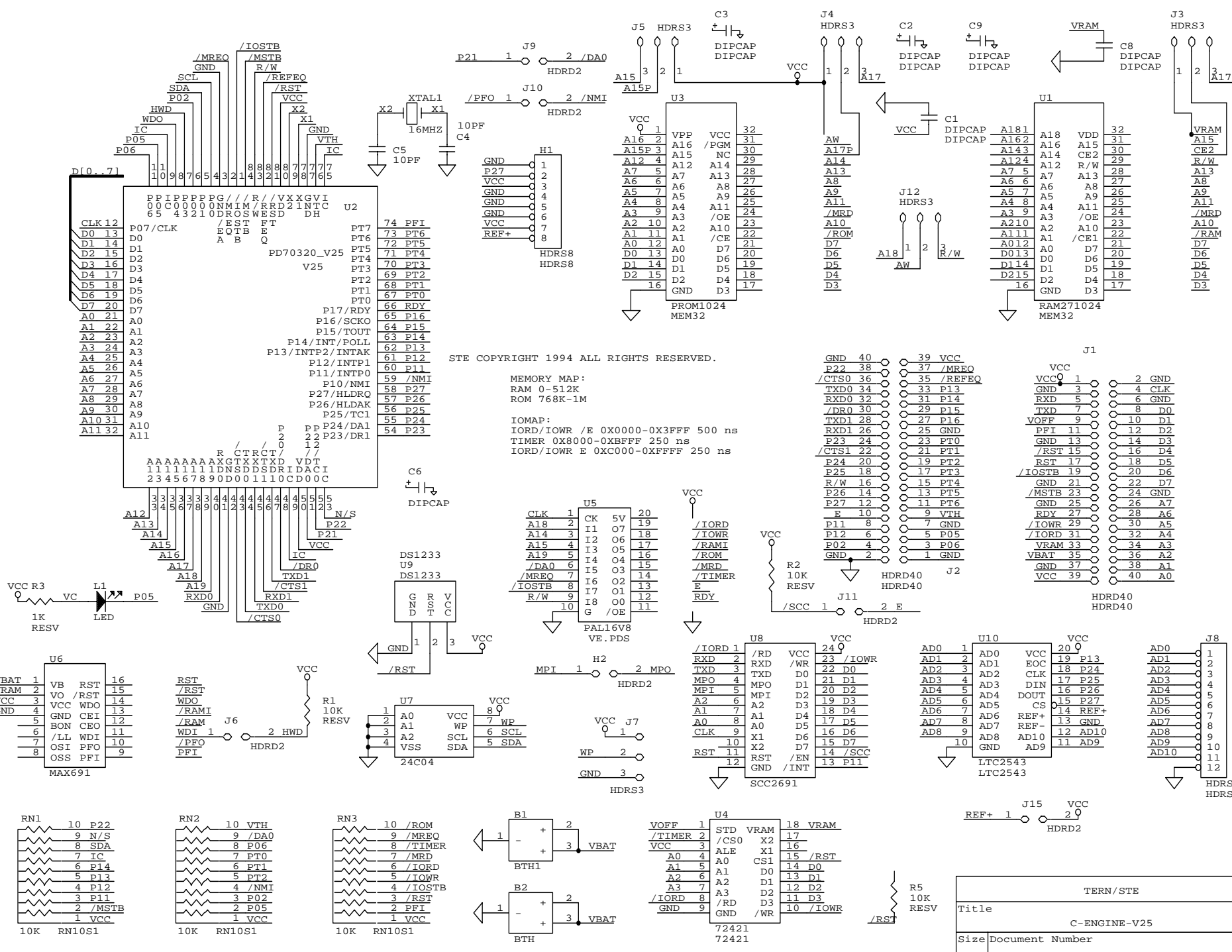


MEMORY MAP:
RAM 0-512K
ROM 768K-1M

IOMAP:
IORD/IOWR /E 0X0000-0X3FFF 500 ns
TIMER 0X8000-0XBFFF 250 ns
IORD/IOWR E 0XC000-0XFFFF 250 ns



| | | |
|-------------------------|-----------------|--------------|
| STE | | |
| Title | | |
| VE-LM | | |
| Size | Document Number | REV |
| B | VELM-MAN.SCH | |
| Date: September 7, 2002 | | Sheet 1 of 1 |



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MEMORY MAP:
RAM 0-512K
RAM 768K-1M

IOMAP:
IORD/IOWR /E 0X0000-0X3FFF 500 ns
TIMER 0X8000-0XBFFF 250 ns
IORD/IOWR E 0XC000-0XFFFF 250 ns

| | | |
|------------------------|-----------------|--------------|
| TERN/STE | | |
| Title C-ENGINE-V25 | | |
| Size | Document Number | REV |
| B | CE-MAN.SCH | |
| Date: January 17, 2000 | | Sheet 1 of 1 |