ACU™

Expansion Card with 16-bit ADCs, CAN, CF, and Ethernet

Technical Manual

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Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

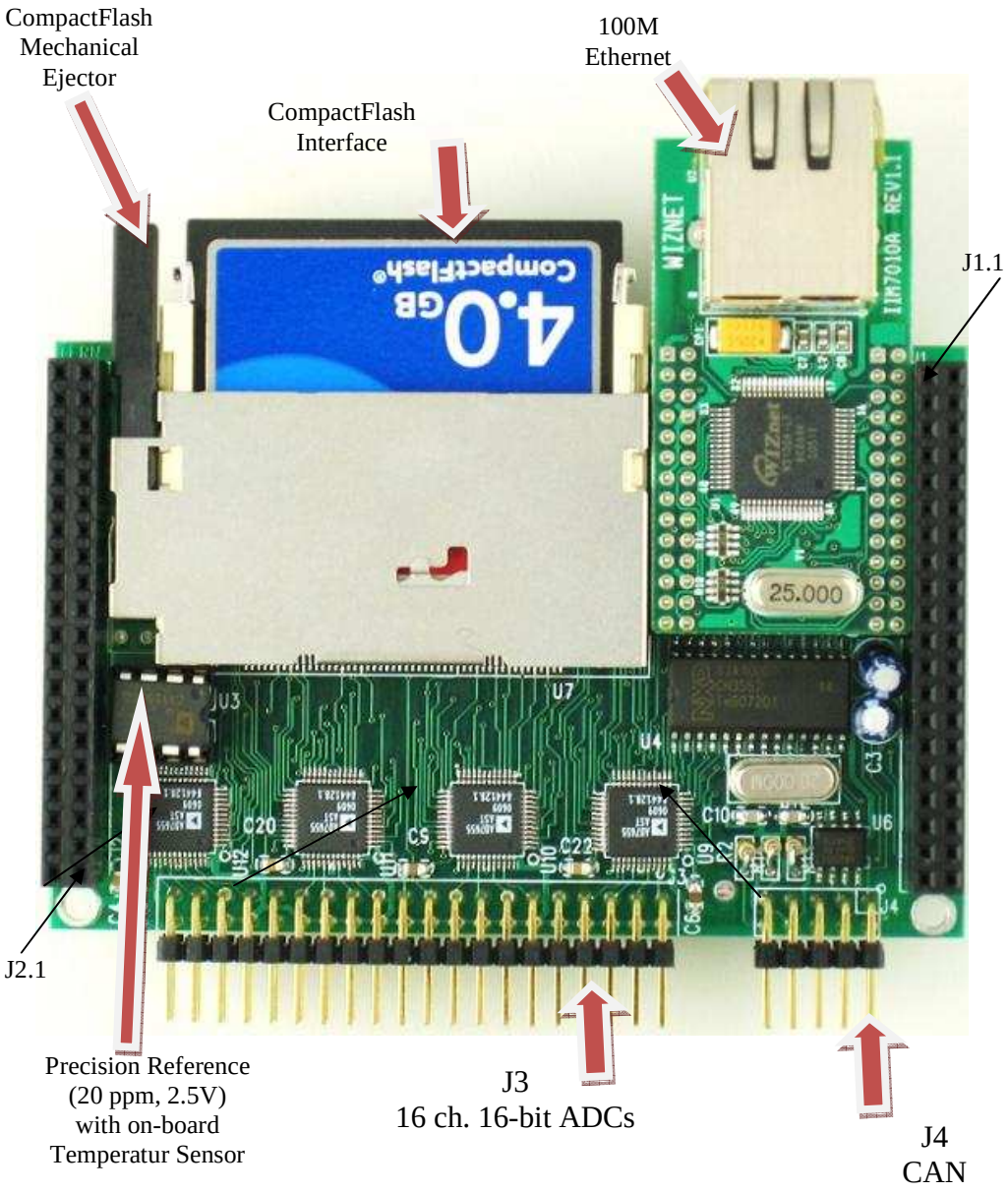
The ***ACU™*** is an expansion card designed for TERN controllers to add high speed 16-bit ADCs, CAN, CompactFlash and Ethernet.
Upto 4 ADC chips (AD7655, 1MHZ, 16-bit, 0-5V□can be installed to provide a total of 16 ADC inputs. Each AD7655 allows *simultaneous* sampling on two channels in hardware. There is a Precision Reference(20 ppm, 2.5V) with on-board Temperature Sensor.

A Controller Aera Network(CAN) controller(SJA1000), running at 20 MHz clock can be installed along with on-board CAN transceiver. It supports up to 1M-bit per second. CAN interrupt and software programmable hardware reset are available. The ***ACU™*** allows TERN controllers directly connect to CAN-bus. All registers of the CAN controller are software accessible.
An Fast Ethernet Module can be installed to provide 100M Base-T network connectivity. This Ethernet module has a hardware LSI TCP/IP stack. It implements TCP/IP, UDP, ICMP and ARP in hardware.
ACU™ allows access to mass storage CompactFlash cards (up to 4GB). Users can easily add mass data storage to their embedded application. Complete C/C++ programmable software package includes compiler, remote debugger, samples, and file system libraries. Files on the CF can be easily accessed from a PC.

1.2 *Features and Options:*

- Measures 3.57 x 2.30 inches
- 16 ch. 16-bit high speed ADC(0-5V, 1MHz, AD7655)
- 100 M Ethernet with hardware TCP/IP stack
- CompactFlash with FAT file system suppot
- CAN bus controller(SJA1000)
- Precision Reference(20 ppm, 2.5V) with on-board Temperature Sensor

Physical Description



Chapter 2: Installation

2.1 Software Installation

Please refer to the Technical manual “Software_Kit.pdf” on TERN CD under tern_docs\manuals\ for installing software and evaluation of TERN controllers.

2.2 Hardware Installation

The ACU is an expansion board built for TERN controllers. The ACU can work with most TERN controllers, including: 586-Engine, 586-Drive, 586-Engine-P, A104, A104S, A-Engine, A-Engine-P, A-Engine86, A-Engine86-P, R-Engine, RA, RD, AE86-D, BirdBox-A, i386-Engine, i386-Engine-P, i386-Engine-L, i386-Engine-M, i386-Drive, SmartLCD, SmartTFT, HD, U-Drive.

Hardware installation for the ACU consists of installing onto its host controller. The ***ACU™*** interfaces with a TERN controller via the J1 and J2 address/data bus. The photo below shows a ACU is installed between a 586-Engine and a P100CAN. The J1 and J2 headers are pass-though all 3 boards.

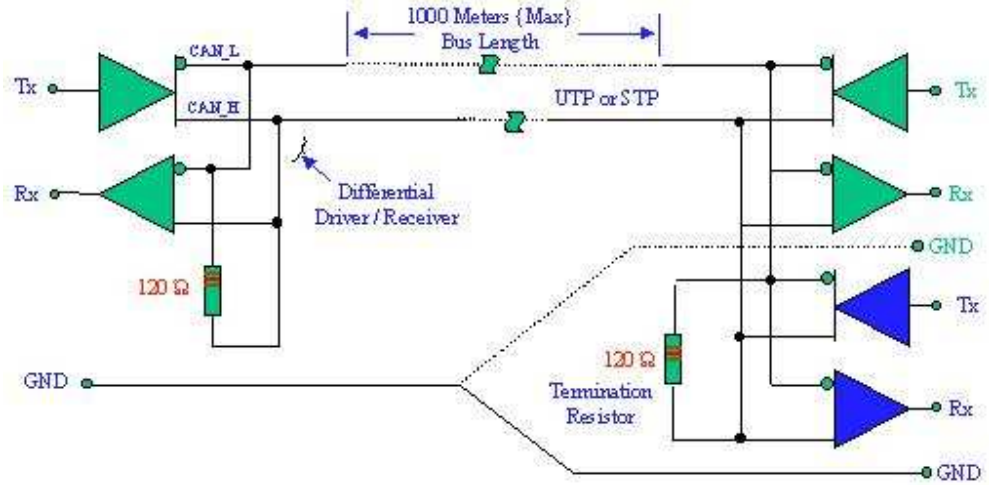
Chapter 3: Hardware / Software

The ACU™ is an expansion board, supporting a CAN bus interface, a 50-pin CompactFlash receptacle, a 100M-T Ethernet Module, 16 channels of 16-bit ADC, and 2 channels of 12-bit DACs.

3.1 CAN(Controller Area Network)

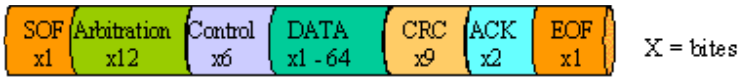
The ACU support an on-board Controller Area Network (CAN) controller(SJA1000, Philips). It supports network baud rates up to 1M-bit per second. Software drivers allow access to all CAN controller registers, as well as a buffering software layer.

The CAN bus is a balanced (differential) 2-wire interface running over either a Shielded Twisted Pair (STP), Un-shielded Twisted Pair (UTP), or Ribbon cable.



CAN Bus Electrical Interface Circuit

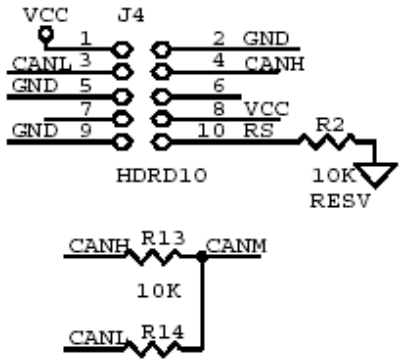
A number of different data rates are defined, with 1Mbps (Bits per second) being the top end, and 10kbps the minimum rate. Cable length depends on the data rate used. Normally all the devices in a system transfer uniform and fixed bit-rates. The maximum line length is 1Km, 40 meters at 1Mbps. Termination resistors are used at each end of the cable. The worst-case transmission time of an 8-byte frame with an 11-bit identifier is 134 bit times (that's 134 microseconds at the maximum baud rate of 1Mbits/sec).



The CAN Bus interface uses an asynchronous transmission scheme controlled by start and stop bits at the beginning and end of each character. This interface is used, employing serial binary interchange. Information is passed from transmitters to receivers in a data frame. The data frame is composed of an Arbitration field, Control field, Data field, CRC field, ACK field. The frame begins with a 'Start of frame' [SOF], and ends with an 'End of frame' [EOF] space. The data field may be from 0 to 8 bits.

The Application for CAN bus includes automotive and industrial field bus. A low speed CAN bus may be employed to operate window and seat controls in a vehicle. A high speed CAN bus may be employed for engine management, brake control, Engine Sensors, and Anti-Skid Systems.

The CAN bus pin out on J4 is shown below. It is a 0.1" spacing 5x2 pin header. User can use a IDE10-DB9 flat cable from TERN to connect CAN signals to an external standard DB9 CAN connector in the field.



A CAN bus transceiver (PCA82C251) is on-board and the RS line is pull down via a SLOPE Control resistor(R2).

For high speed operation, the R2 is zero ohm, the transmit output is switched ON/OFF as fast as possible, and no measures are taken to limit the rise and fall slope. In this mode, shield cable is recommended to avoid RFI problems.

While in slope control mode with R2 installed, the rise and fall slope is limited and a flat cable can be used.

Sockets for R13 and R14 allow user to install CAN bus termination resistors.

3.2 50-pin CompactFlash Interface

A 50-pin CompactFlash receptacle can be installed on the ACU and also a mechanical ejector.

It supports 50-pin mass storage CompactFlash cards with Windows compatible FAT file system support, allowing user easily transfer large amounts of data to or from a PC.

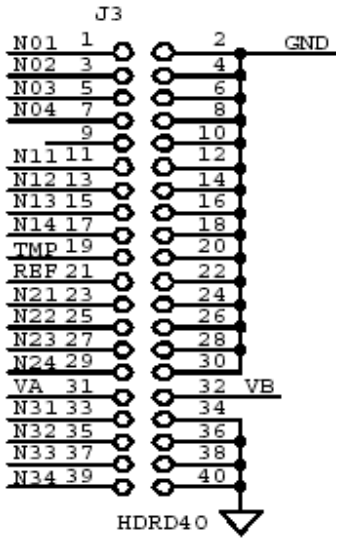
3.3 Ethernet

An WizNet™ Fast Ethernet Module can be installed to provide 100M Base-T network connectivity. This Ethernet module has a hardware LSI TCP/IP stack. It implements TCP/IP, UDP, ICMP and ARP in hardware, supporting internet protocol DLC and MAC. It has 16KB internal transmit and receiving buffer which is mapped into host processor's direct memory. The host can access the buffer via high speed DMA transfers. The hardware Ethernet module releases internet connectivity and protocol processing from the host processor. It supports 4 independent stack connections simultaneously at a 4Mbps protocol processing speed. An RJ45 8-pin connector is on-board for connecting to 10/100 Base-T Ethernet network. A software library is available for Ethernet connectivity.

3.4 AD7655, 16-bit parallel high speed ADC

The unique 16-bit parallel ADC (AD7655, 0-5V) supports ultra high-speed (1 MHz conversion rate) analog signal acquisition. The ACU can support up to 4 AD7655 chips for a total of 16 ADC inputs. Each AD7655 contains two low noise, high bandwidth track-and-hold amplifiers that allow *simultaneous*

sampling on two channels. Each track-and hold amplifier has a multiplexer in front to provide a total of 4 channels analog inputs on each ADC chip. The parallel ADC achieves very high throughput by requiring only two CPU I/O operations (one start, one read) to complete a 16-bit ADC reading. With a precision external 2.5V reference, the ADC accepts 0-5V analog inputs at 16-bit resolution of 0-65,535.
The ADC input signals are routed on header J3:



See sample program \tern\586\samples\acu\acu_ad.c for details on reading the ADC. The sample program is also included in the pre-built sample project; \tern\586\samples\acu\acu.ide.
Refer to the data sheet for additional specifications; \tern_docs\parts\ad7655.pdf.

3.5 DAC (LTC1446)

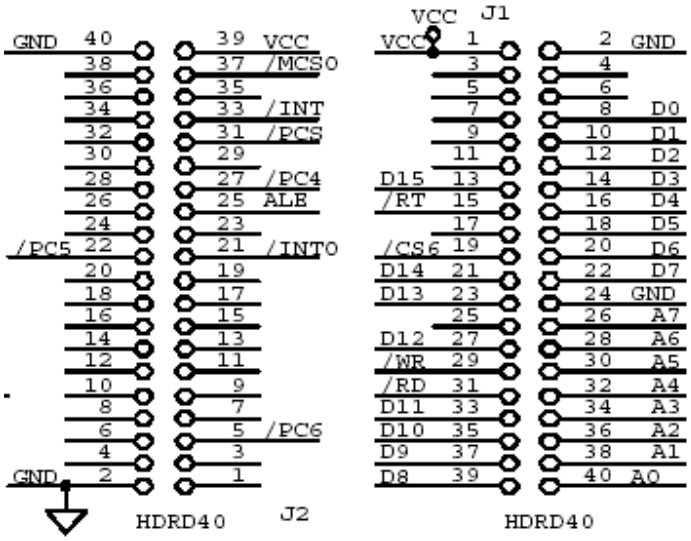
The LTC1446/LTC1446L is a dual 12-bit digital-to-analog converter (DAC) in an SO-8 package. It is complete with a rail-to-rail voltage output amplifier, an internal reference and a 3-wire serial interface. The LTC1446 outputs a full-scale of 4.096V, making 1 LSB equal to 1 mV. The LTC1446L outputs a full-scale of 2.5 V, making 1 LSB equal to 0.61 mV.

The buffered outputs can source or sink 5 mA. The outputs swing to within a few millivolts of supply rail when unloaded. They have an equivalent output resistance of 40 Ω when driving a load to the rails. The buffer amplifiers can drive 1000 pf without going into oscillation.

The DAC can be installed in U14 on the ACU, and the outputs are routed to J3 pin 31 for DAC channel A(VA), and J3 pin 32 for DAC channel B(VB).

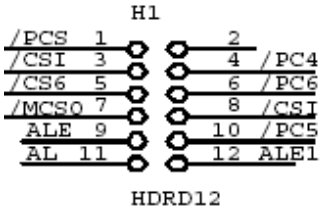
3.6 Interface to TERN host controller via J1 and J2

The ACU is designed to interface to a host TERN controller via two 20x2 pin headers. All high speed address, data, and control lines are located on J1. Many PIO lines, interrupt line, and chip select lines are on J2.



The signal names on J1 and J2 pin headers may be different on different host controllers, such as 586E, i386E, AE86. User needs to find out the active signal names and functions based on the location or the pin number on the J1 and J2 header of the host controller.

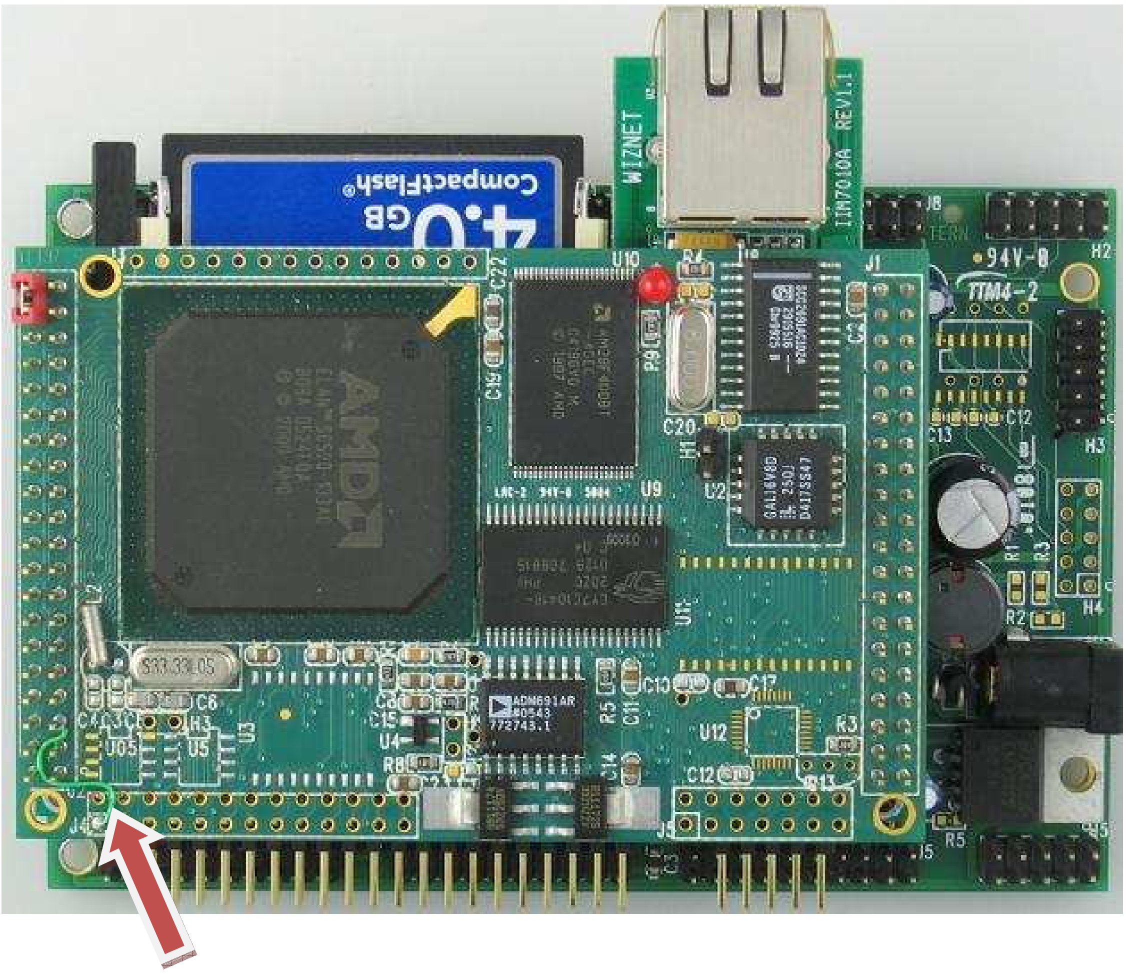
3.7 Chip Selects and Hardware Configuration Header



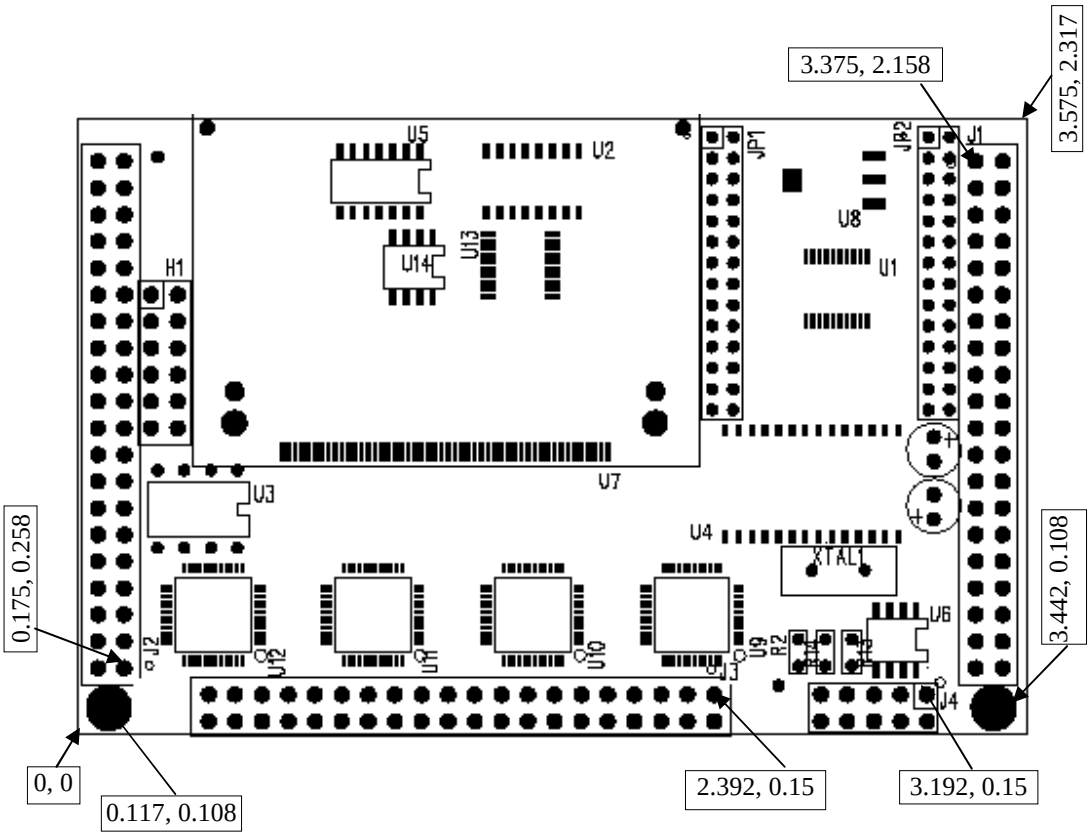
In order to allow the ACU to work with most of the TERN host controllers in different combinations, a hardware configuration header is on board. By default, H1 pin 6=pin 8, also pin11=pin12 are connected by trace.

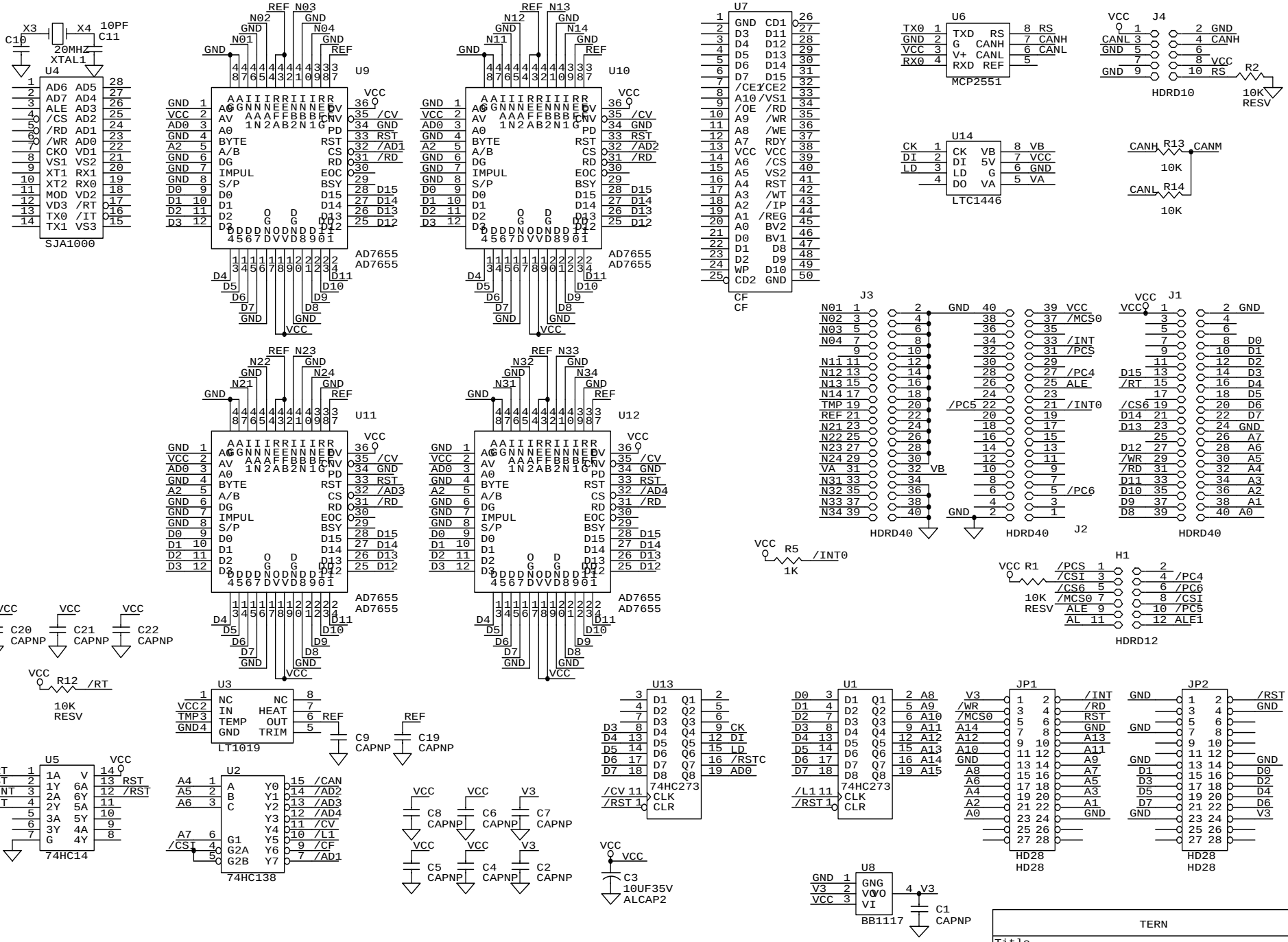
As an example, a 586-Engine, an ACU, and a P100CAN boards are assembled as shown in the photo below. This system can provide 586 CPU, 16 channels of 16-bit ADC, 8 channels of 12-bit ADC, 100+ I/O lines, CompactFlash, 100M Ethernet, RS232, RS485 and two independent CAN interfaces.

In order to select P100CAN and ACU in the same system by an 586-Engine, a wire jumper, from J4.1 to J2.5, must be added to provide an extra chip select line (/GPCS3).


CompactFlash
4.0GB
WIZNET
IIM7010A REV1.1
AMD
ADM691AR
94V-0
TTM4-2

ACU Layout Dimensions




X3
X4
10PF
C10
C11
20MHZ
XTAL1
U4
SJA1000
REF N03
U9
REF N13
U10
U7
CF
U6
MCP2551
J4
HDRD10
10K
RESV
U14
LTC1446
CANH R13 CANM
10K
CANL R14
10K
REF N23
U11
REF N33
U12
J3
HDRD40
J2
HDRD40
J1
HDRD40
VCC R5 /INT0
1K
H1
HDRD12
C20 CAPNP
C21 CAPNP
C22 CAPNP
VCC R12 /RT
10K
RESV
U3
LT1019
C9 CAPNP
C19 CAPNP
U5
74HC14
U2
74HC138
C8 CAPNP
C6 CAPNP
C7 CAPNP
C5 CAPNP
C4 CAPNP
C2 CAPNP
U13
74HC273
U1
74HC273
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HD28
JP2
HD28
C3
10UF35V
ALCAP2
U8
BB1117
C1
CAPNP
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Date:
March 21, 2008
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