GR4™

Multichannel, High-Speed, Simultaneous Sampling 16-bit ADC

Technical Manual

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Chapter 1: Hardware

1.1 Functional Overview

The GR4™ is a multi-channel high speed 16-bit analog signal acquisition board, designed as an expansion for TERN programmable controllers. Four stacked GR4 units can continuously acquire and store 8 analog signals into CompactFlash cards for hours at 8MB of data per second.

The GR4™ implements multi-channel data acquisition in hardware. It can start conversions across multiple channels of ADC simultaneously, pushing 16-bit data into FIFO memory and then stop when the FIFO buffer is full. Sampling on a second pair of ADC can be triggered upon completion of sampling on the first chip. Thus, while the hardware is sampling on one ADC chip to its FIFO, the host CPU can start moving data from the other ADC FIFO buffer into CompactFlash card.

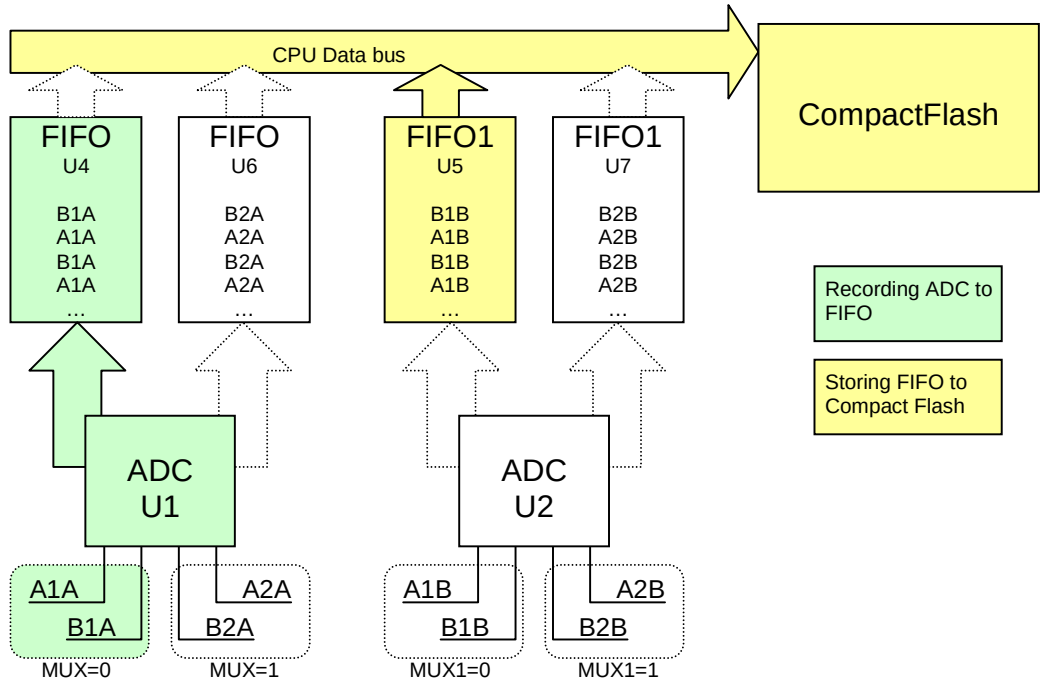


Figure 1.1 GR4 acquiring and storing 16-bit ADC readings

1.2 High Speed 16-bit ADC (AD7655)

The unique 16-bit parallel ADC (AD7655, 0-5V) supports ultra high-speed (1 MHz conversion rate) analog signal acquisition. The AD7655 contains two low noise, high bandwidth track-and-hold amplifiers that allow simultaneous sampling on two channels. Each track-and hold amplifier has a multiplexer in front to provide a total of 4 channels analog inputs. The parallel ADC achieves very high throughput by requiring only two I/O operations (one start, one read) to complete a 16-bit ADC reading. With a precision external 2.5V reference, the AD7655 accepts 0-5V analog inputs at 16-bit resolution, yielding 65536 counts/5000mV = 13 LSB/ mV.

1.3 Control and Status Lines

GR4 operations are controlled by five control lines and one status line: AD, RT, AST, TR, MUX and SA. The table below describes the control and status lines for the GR4. Units with two ADCs use the additional control and status lines AD1, RT1, AST1, TR, MUX1 and SB that perform the same function on the second ADC/FIFO set.

Signal	Description	Signal High	Signal Low
AD	Chip enable for ADC	ADC disabled, CPU can read FIFO	ADC enabled, can write to FIFO
RT	Chip reset for ADC	Resets ADC AD7655	ADC AD7655 normal operation
AST	Chip reset for counter	Resets counter to address 0	Counter active
MUX	Addr select for ADC	Select ADC channel A2 and B2	Select ADC channel A1 and B1
TR	External trigger	Starts ADC-FIFO recording	Stops ADC-FIFO recording
SA	FIFO status	FIFO is full, recording complete	ADC to FIFO recording in progress

Table 1.1 GR4 Control and Status Lines

1.4 FIFO Memory Size

Header H3 selects the memory size of FIFO and FIFO1. H3 ties the upper FIFO address bit to SA and SB causing the recording to stop when the end of the FIFO is reached. The figure below shows how to set H3.

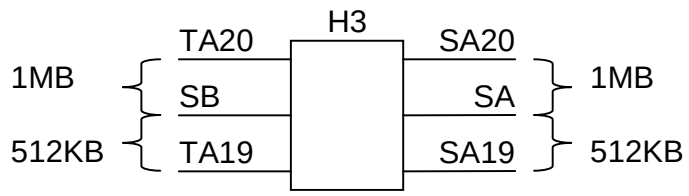


Figure 1.2 FIFO Size Settings

1.5 Recording ADC to FIFO

By default, the GR4 comes with one AD7655 ADC, two 512KB FIFOs and a CompactFlash receptacle. With this configuration, analog data from two of the four channels can be sampled and stored into one of the two FIFOs. ADC reading are read and stored in the FIFO automatically. No action from the CPU is needed once recording has started. When the FIFO is full, recording will halt. Samples from the ADC will alternate between input A and B. First input B will record then input A. When recording has completed, SA will go high (SA=1) and the data can be copied from the FIFO to the onboard CompactFlash.

Perform the following actions to record ADC samples to the FIFO:

Set the MUX. MUX=0 for A1/B1, MUX=1 for A2/B2

Enable the AD7655 ADC. AD=0

Reset the counter. AST=1

Enable counter to begin recording. AST=0

Poll the FIFO status. While SA=0, the FIFO is recording. When SA=1, recording is complete.

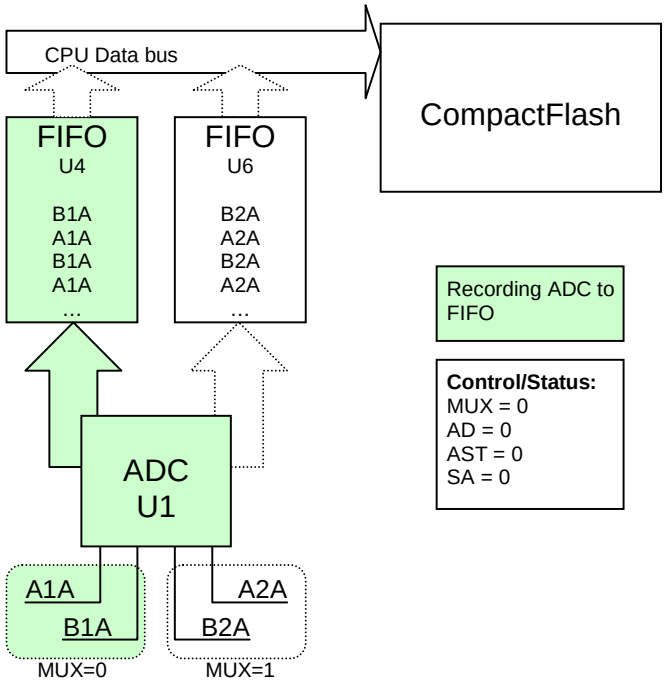


Figure 1.3 Recording ADC Channel 1 to FIFO.

1.6 Storing FIFO to Compact Flash

When the FIFO is full, the CPU can transfer the data to the onboard CompactFlash. The CPU can manually transfer the data in software or use DMA to transfer data in hardware (see sample program gr4_cf.c). To do so, the AD7655 ADC must be disabled and the counter reset. With AD=1 (ADC disabled), each read from the FIFO will increment the counter for the next stored value to be read. The raw 16-bit data is stored on the CF card starting from sector 0 to sector 0x1000000 for an 8GB CF card. Each sector is 512 bytes. With a FIFO size of 512KB (1024 sectors), sectors 0-1023 store data from the 1st ADC, and sectors 1024-2047 store data from 2nd ADC. Data stored in the FIFO alternates between channel A and B of the ADC. This will also be true when transferred to the CompactFlash.

Perform the following actions to read the FIFO:

Set the MUX. MUX=0 for A1/B1, MUX=1 for A2/B2

Disable the AD7655 ADC. AD=1

Reset the counter. AST=1

Enable counter. AST=0

Continue reading until all data has been read. When SA=1, reading FIFO complete.

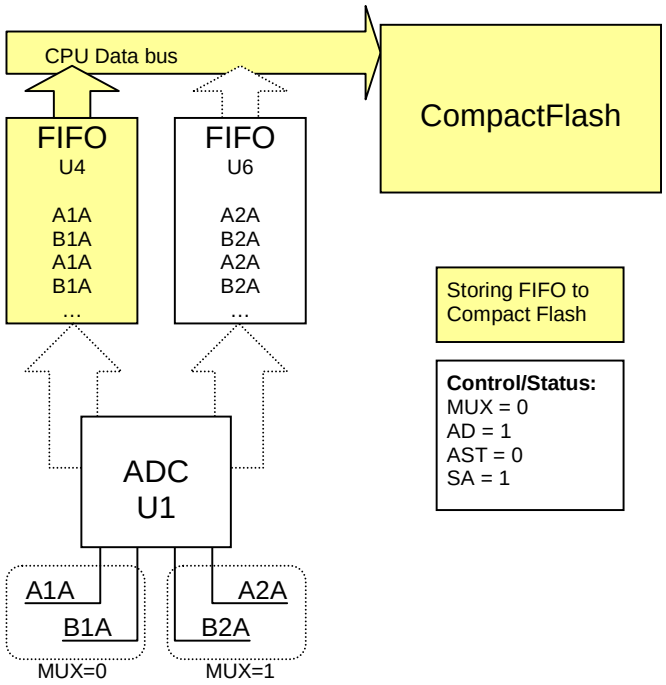


Figure 1.4 Storing FIFO data to CompactFlash.

1.7 GR4 with second AD7655 ADC and FIFO

The operation for using the optional second ADC and FIFO is the same for using one. With the additional ADC/FIFO, analog readings can be recorded in one FIFO while data from the other FIFO is transferred to CompactFlash. This allows for continuous analog recording without interruption until the CompactFlash is full. Hardware triggers TR and TR1 are provided to allow instantaneous switching from recording on FIFO to FIFO1. ADC recording starts as soon as TR goes high, and stops when TR goes low. The same rules apply for TR1. Connection TR=SB and TR1=SA will cause automatic switching between the FIFOs. When FIFO completes recording, SA will go high, forcing TR1 high which causes FIFO1 to start recording.

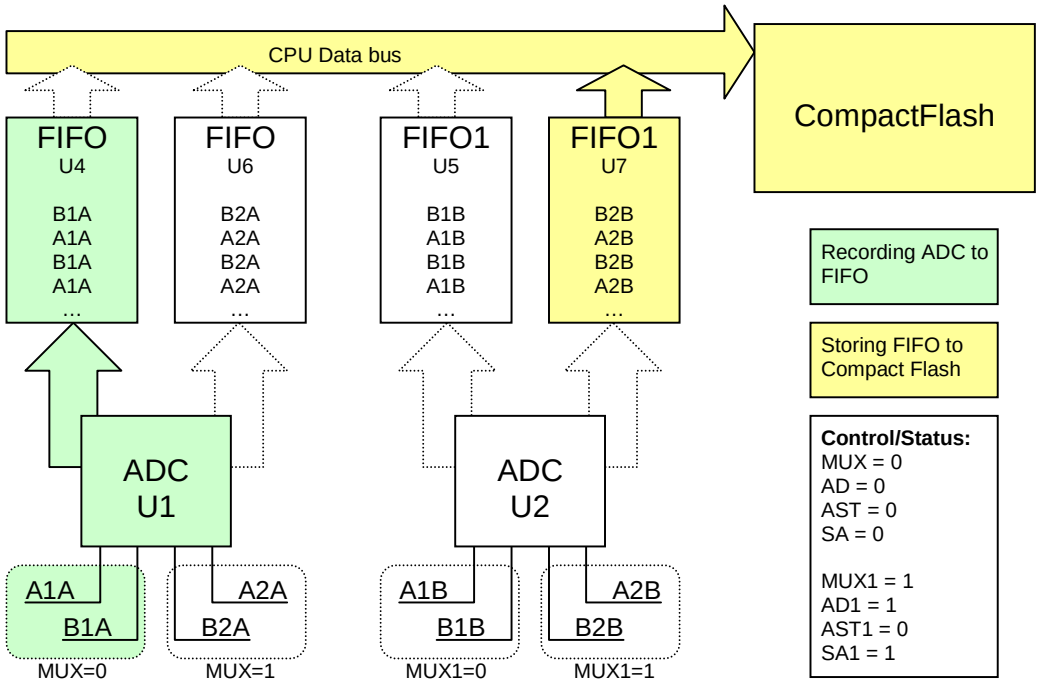


Figure 1.5 Storing FIFO data to CompactFlash.

1.8 Stacking Multiple GR4's

Four GR4 units can be stacked to increase analog inputs and data storage. Four stacked GR4 units can continuously acquire and store 8 analog signals into CompactFlash cards for hours at 8MB of data per second. Four PALs are available for stacking four GR4s with one chip select: GR4100, GR4140, GR4180, and GR41C0. See sample ***samples\gr4\gr4_cf.c*** for reading from four GR4s.

Figure 1.6 Four Stacked GR4s

1.9 ADC Conversion Clock

The sample rate is based on a conversion clock which can be from an on-board oscillator or an external clock. The maximum conversion clock is 500 KHz. Each conversion clock can record up to four channels of 16-bit ADC data from two AD7655 chips on each GR4 board. A stack of four GR4s can share the same external conversion clock.

Header H1 selects the conversion clock CV. When H1.1 = H1.2, the GR4 uses an external clock from J2.29 = P1 as the conversion clock. P1 is the user programmable controller timer output from the host controller. When H1.2 = H1.3, the GR4 uses an onboard clock signal from an optional oscillator at K1.

With a 500 KHz clock, the GR4 can simultaneously record four analog signals on FIFO 500,000 times per second with 16-bit resolution. Alternately, the GR4 with a 500 KHz clock can record two analog signals simultaneously while storing the other two onto a CompactFlash 500,000 times per second. At 2MB of data per second, a GR4 with an 8GB CompactFlash card can record: 8,000MB / 2MB = 4000 seconds = 1.11 hours of uninterrupted analog data. Stack four GR4s to record 4.44 hours of data. Use four GR4s with 32GB CompactFlash cards and record for over 17 hours!

1.10 Headers and Connectors

1.10.1 Headers J1 and J2

Headers J1 and J2 connect to the host controller like AE, AE86 or 5E.

J2 Header			
GND	40	39	VCC
	38	37	
	36	35	
	34	33	
	32	31	/RTS1
	30	29	P1
	28	27	
	26	25	
	24	23	
/CTS1	22	21	
	20	19	
	18	17	
	16	15	
	14	13	
	12	11	
	10	9	
	8	7	
	6	5	
	4	3	
	2	1	

J1 Header			
VCC	1	2	GND
	3	4	CLK
	5	6	
	7	8	D0
	9	10	D1
	11	12	D2
D15	13	14	D3
/RST	15	16	D4
	17	18	D5
P16	19	20	D6
D14	21	22	D7
D13	23	24	GND
	25	26	A7
D12	27	28	A6
/WR	29	30	A5
/RD	31	32	A4
D11	33	34	A3
D10	35	36	A2
D9	37	38	A1
D8	39	40	A0

1.10.2 Header J3

Header J3 provides access to the 8 analog inputs.

J3 Header			
SA	1	2	TR1
GND	3	4	A2B
GND	5	6	B2B
GND	7	8	A1B
GND	9	10	B1B
GND	11	12	A2A
GND	13	14	B2A
GND	15	16	A1A
GND	17	18	B1A
SB	19	20	TR

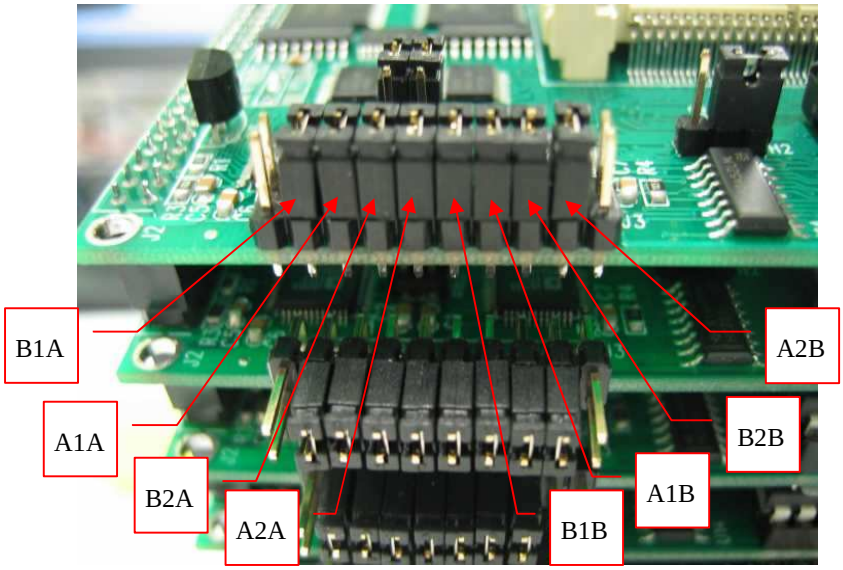


Figure 1.7 Analog Inputs Jumpered to Ground at J3

Header H3

Header H3 selects the FIFO size. See figure 1.2 for configuration.

H3 Header			
TA20	1	2	SA20
SB	3	4	SA
TA19	5	6	SA19

1.10.3

1.10.4 Header H1

Header H1 selects the conversion clock CV.

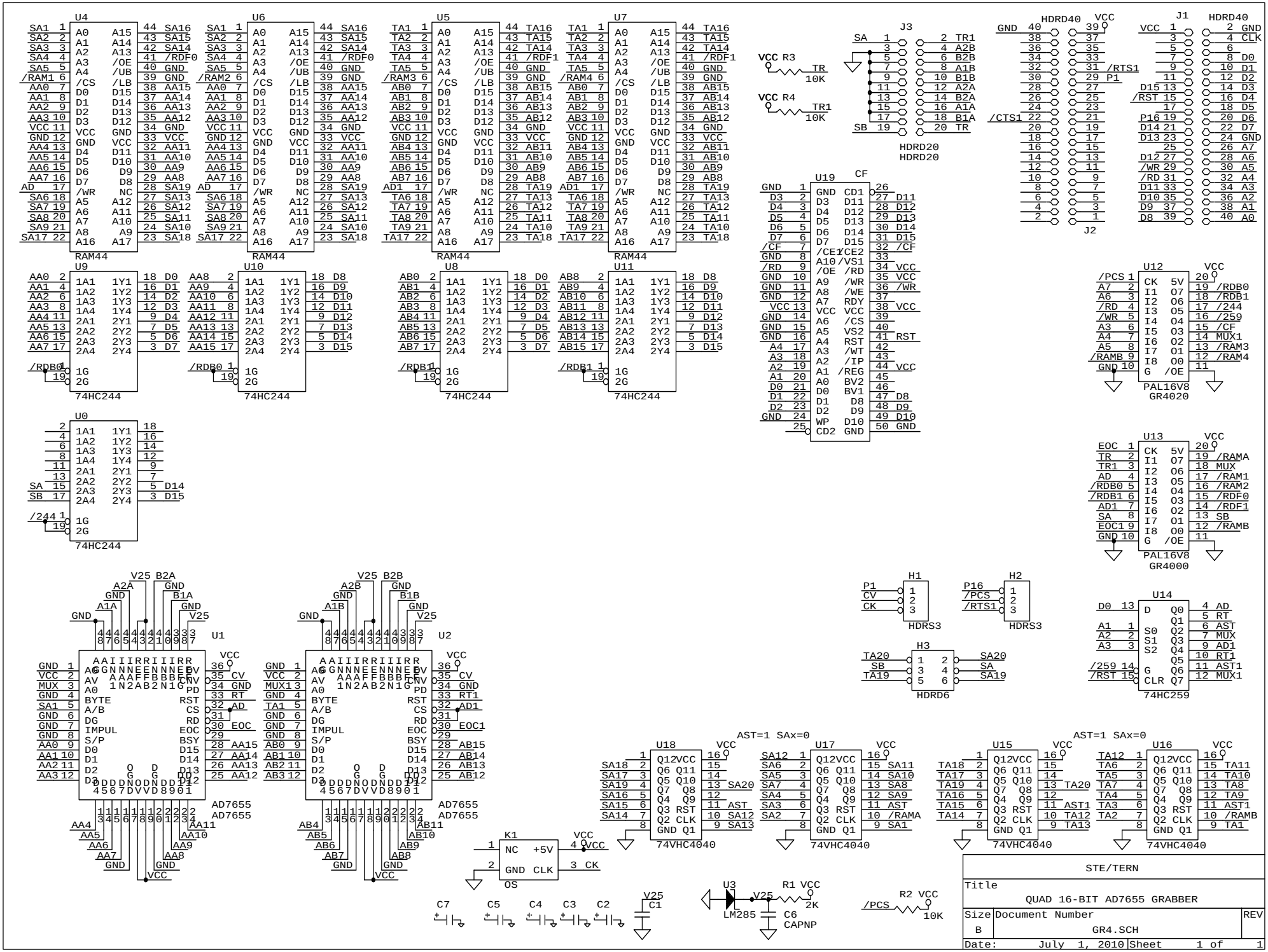
H1 Header	
1	P1
2	CV
3	CK

1.10.5

1.10.6 Header H2

Header H2 sets the chip select (/PCS) for the GR4. When H2.1=H2.2, /PCS=P16=J1.19. When H2.2=H2.3, /PCS=/RTS1=J2.31. See the GR4 sample programs for the correct chip select settings.

H2 Header	
1	P16
2	/PCS
3	/RTS1


U4
U6
U5
U7
RAM44
U9
U10
U8
U11
74HC244
U0
U1
U2
AD7655
J3
HDRD20
J2
HDRD40
J1
U19
CF
PAL16V8
GR4020
U12
GR4000
U13
H1
H2
H3
HDRS3
HDRD6
U14
74HC259
U18
U17
U15
U16
74VHC4040
AST=1 SAx=0
K1
OS
U3
LM285
R1 VCC
2K
C6
CAPNP
R2 VCC
10K
R3
R4
STE/TERN
QUAD 16-BIT AD7655 GRABBER
GR4.SCH
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