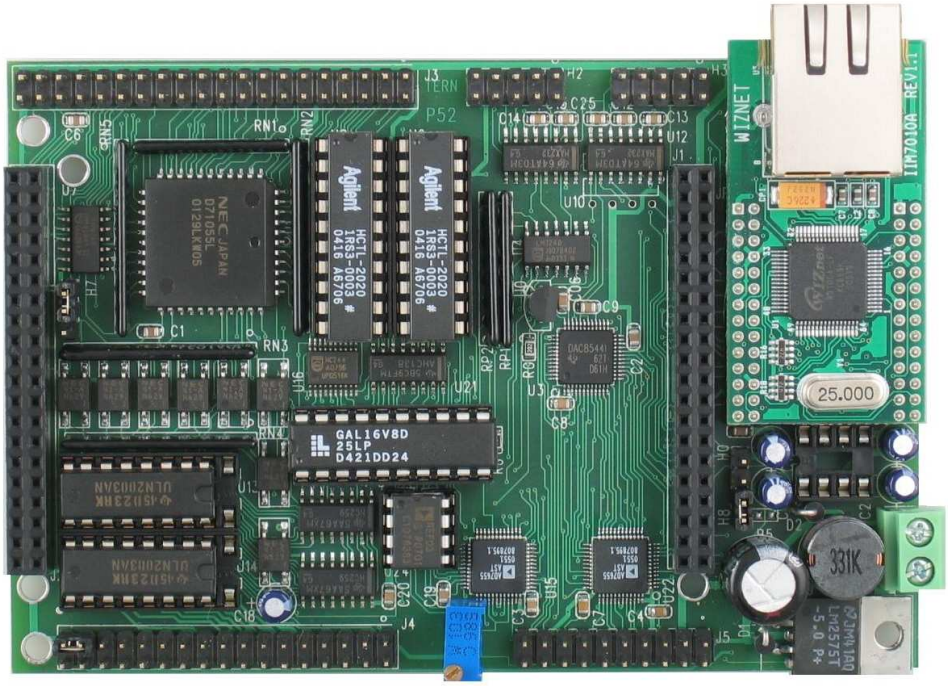
P52™

I/O expansion card with ADC, DAC, 24 PPI I/Os, 100M BaseT Ethernet, Quadrature Decoders, RS232/485



Technical Manual

TERN INC.
1950 5th Street, Davis, CA 95616, USA
Tel: 530-758-0180 Fax: 530-758-0181
Email: sales@tern.com http://www.tern.com

Version 2.00

November 2, 2010

1950 5th Street, Davis, CA 95616, USA
Tel: 530-758-0180 Fax: 530-758-0181
Email: ***sales@tern.com*** ***http://www.tern.com***

Important Notice

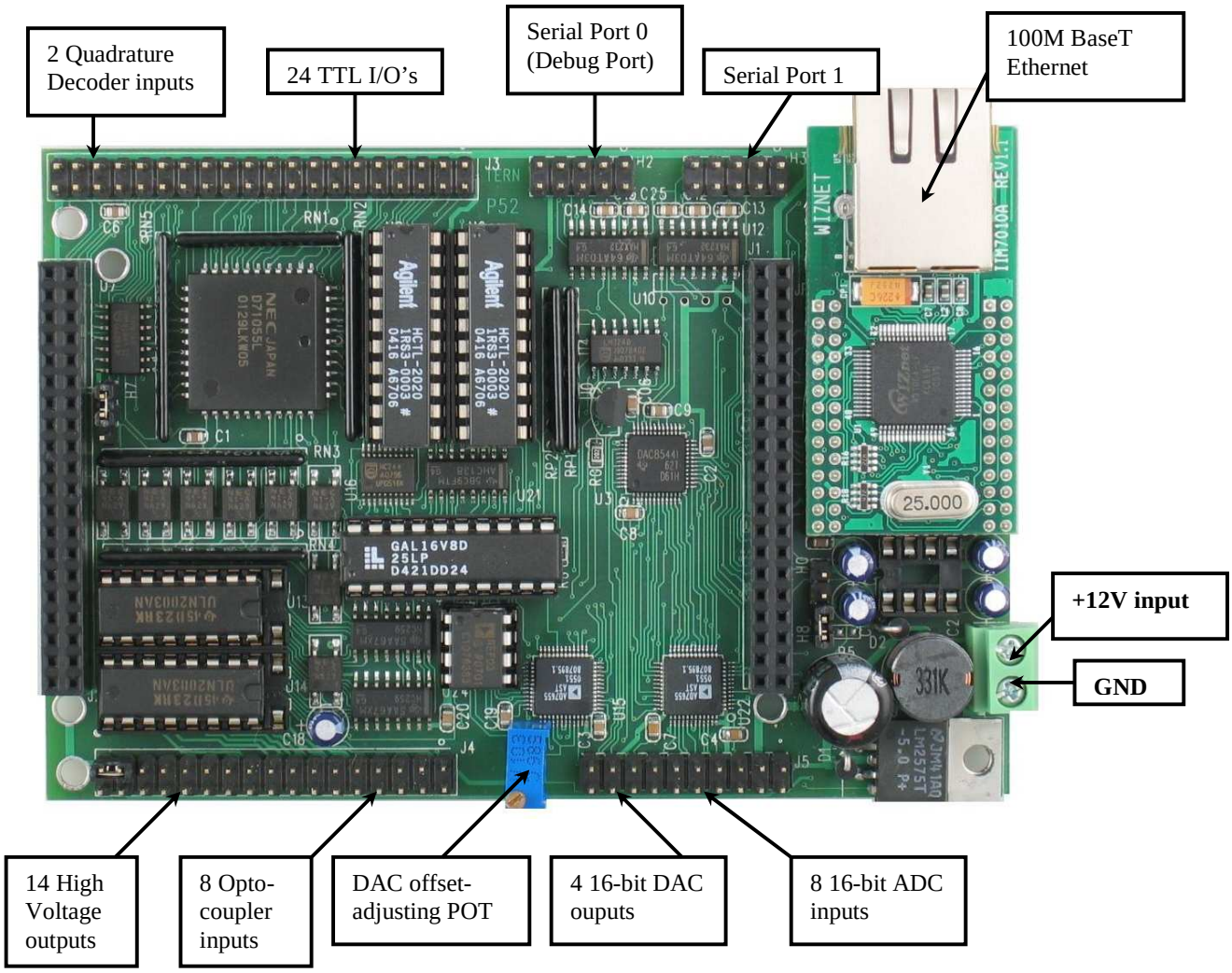
TERN is developing complex, high technology integration systems. These systems are integrated with software and hardware that are not 100% defect free. ***TERN products are not designed, intended, authorized, or warranted to be suitable for use in life-support applications, devices, or systems, or in other critical applications. TERN*** and the Buyer agree that ***TERN*** will not be liable for incidental or consequential damages arising from the use of ***TERN*** products. It is the Buyer's responsibility to protect life and property against incidental failure.
TERN reserves the right to make changes and improvements to its products without providing notice.
Temperature readings for controllers are based on the results of limited sample tests; they are provided for design reference use only.

Chapter 1: Introduction

1.1 Functional Description

Measuring 4.4 x 3.1 inches, the ***P52*** is an I/O expansion board designed for and driven by a Tern host controller. A 16-bit external data bus is required to run the parallel ADC and DAC on the ***P52***. Many embedded applications demand high speed ADC and DAC with buffered operational amplifiers supporting variable gains or offset for analog signals. The ***P52*** supports four 16-bit, parallel DACs (DAC8544) buffered by 4 ops with gain=2 (hardware adjustable), providing ±5V analog output by default. A resistor pot is used to adjust the DAC analog output offset. It also supports eight 16-bit parallel ADC inputs (AD7655).

The ***P52*** can buffer PIOs with 16 sourcing drivers (UDN2982), or 14 sinking drivers (ULN2003). These drivers can source or sink 350 mA at 50V per line to directly drive solenoids, relays, or lights. Eight high isolation voltage photocouplers (PS2701, NEC) can be installed to provide optically isolators to PIOs. Two quadrature decoders, (HCTL2020, Hewlett Packard) can be installed to interface incremental motion encoders. In addition, 24 bi-directional TTL PPI I/Os (82C55) are software programmable and free to use.



A 100M BaseT Ethernet controller (Wiznet) can be installed to provide network connectivity. A software stack library is available, supporting network protocols like ARP, DHCP, UDP, ICMP, and of course TCP over the Ethernet network.

Two channels of RS-232 drivers and a 5V linear regulator are on-board. An optional RS232 or RS485 driver can be installed for the optional 3rd UART of the host controller. The ***P52*** requires 8.5V to 12V DC power supply with linear regulator, or up to 30V DC power input with an optional switching regulator without generating excessive heat.

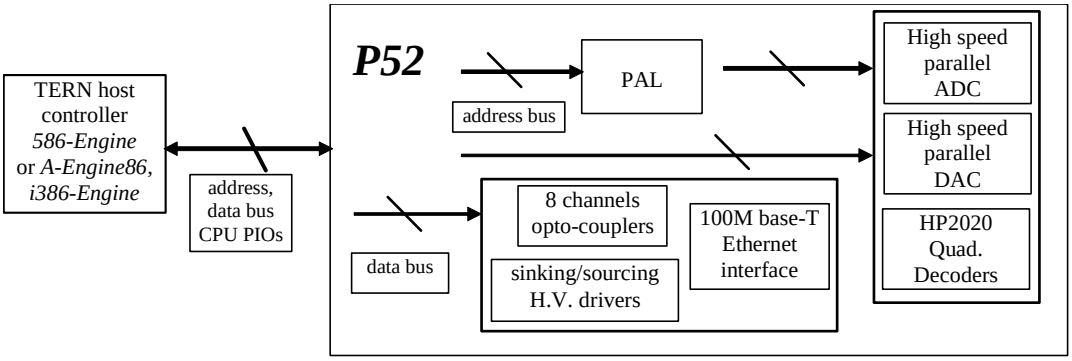


Figure 1.1 Functional block diagram of the P52

1.2 Features

- ► 4.4x3.1x0.5 inches.
- ► Driven by ***586-Engine™*** , ***i386-Engine™, A-Engine86™***.
- ► Power consumption: < 200 mA @ 9V-12V
- ► 2 channels RS-232 serial communication
- ► 24 PPIs, 14 high voltage sourcing or sinking drivers
- ► Wiznet 100M Base-T Ethernet Controller
- ► 8 ch. 16-bit ADC(AD7655) x 2
- ► 4 ch. 16-bit DAC (DAC8544) with buffer ops*.
- ► 8 opto-isolators and 2 quadrature decoders*
- ► 5V switching regulator*
- ► RS-232/485 for optional 3rd UART on controlling 'Engine'*

*optional

Chapter 2: Installation

2.1 Connecting the P52 and the host 'Engine' to the PC

Using P52 COM Ports:

The following diagram (Figure 2.1) illustrates the connection between the ***P52*** and the PC via a serial cable.

A host controller must be installed on the ***P52*** via J1 and J2 headers ***before power on***. The host communicates through SER0 for debugging by default. Thus, the 5x2 IDC connector must be installed on the SER0 of the ***P52*** (header H2). ***IMPORTANT:*** *Note that the* ***red*** *side of the cable must point to pin 1 of the H2 header*. The DB9 connector should be connected to one of your PC's COM Ports (COM1 or COM2).

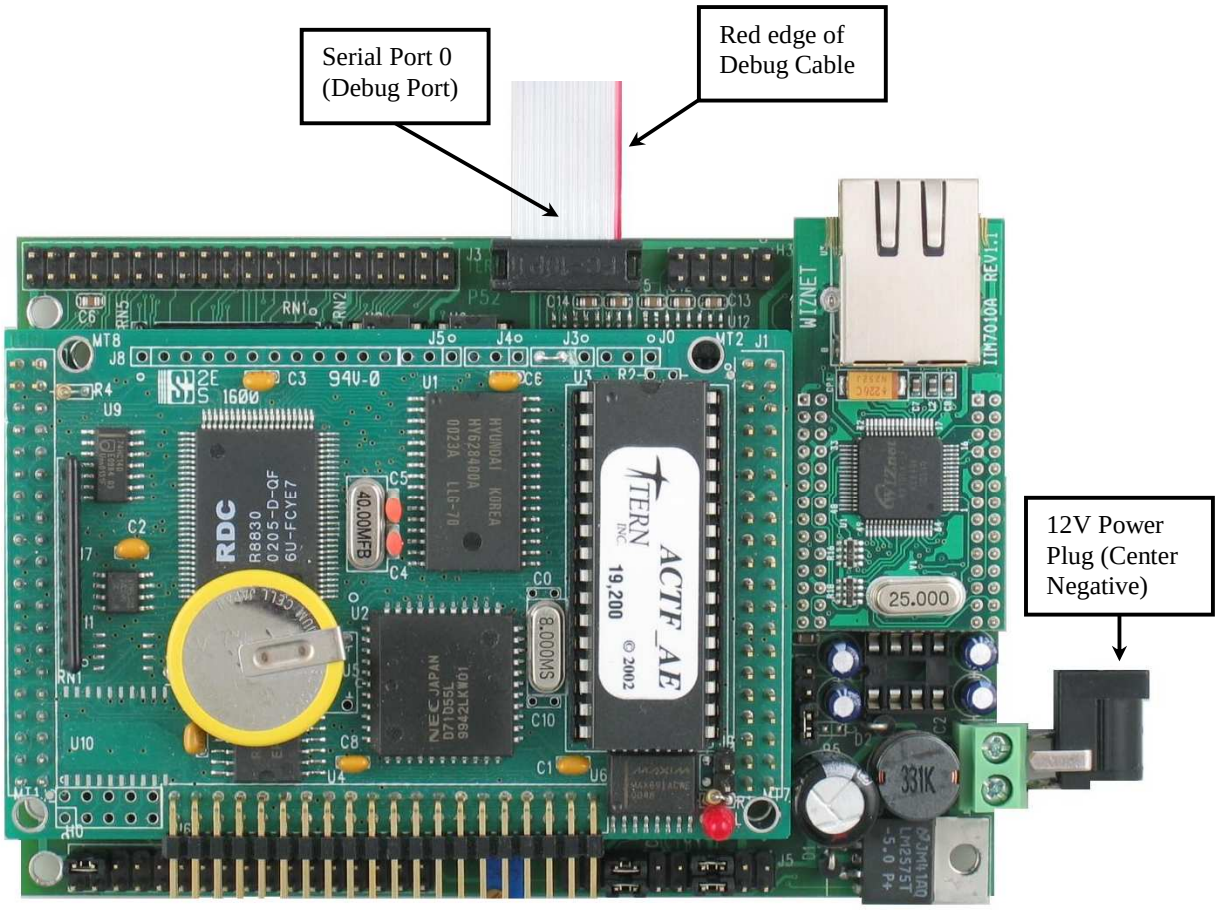


Figure 2.1 P52 driven by host controller **A-Engine-40**

Using Host Controller COM ports:

In the case where the host controller already provides Serial Ports 0 and 1, such as the **5P** shown below, ***P52*** header H2 (Ser 0) will be blocked off. To negotiate with this change, we can use the debug port (Ser 0) on the host controller and avoid Serial ports 0 and 1 on the ***P52,*** as shown below with the **5P** as host.

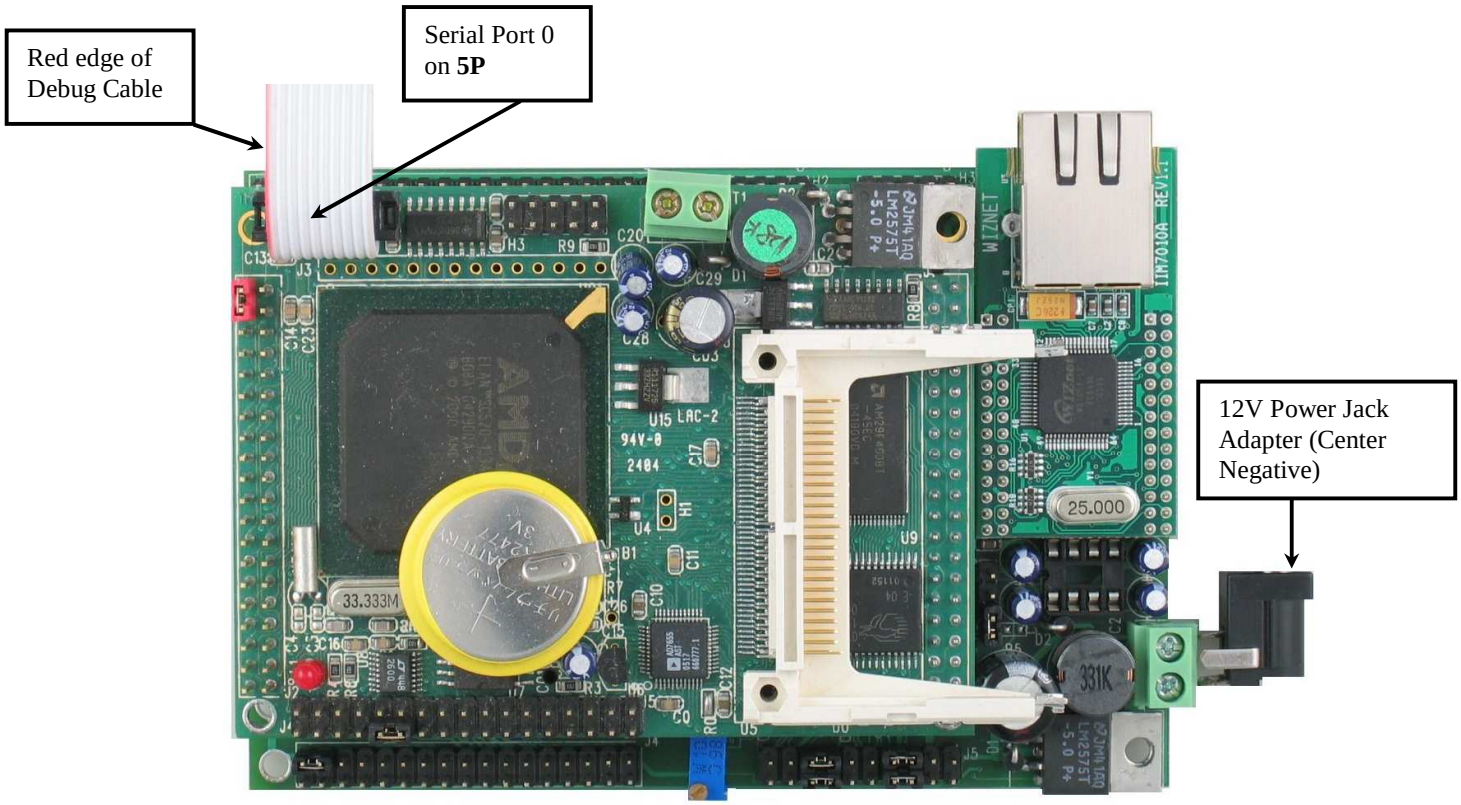


Figure 2.2 P52 driven by host controller **586-Engine-P**.

The ***P52*** must be powered by an unregulated +12 Volts (or up to +30V with an optional switching regulator). A 2x1 screw terminal is installed to accept this +12V input. See schematic for orientation of screw terminal. Using the power jack adapter provided with a TERN EV-P or DV-P Kit, connect the output of the wall transformer to your ***P52*** (as seen in above diagram).

Chapter 3: Hardware

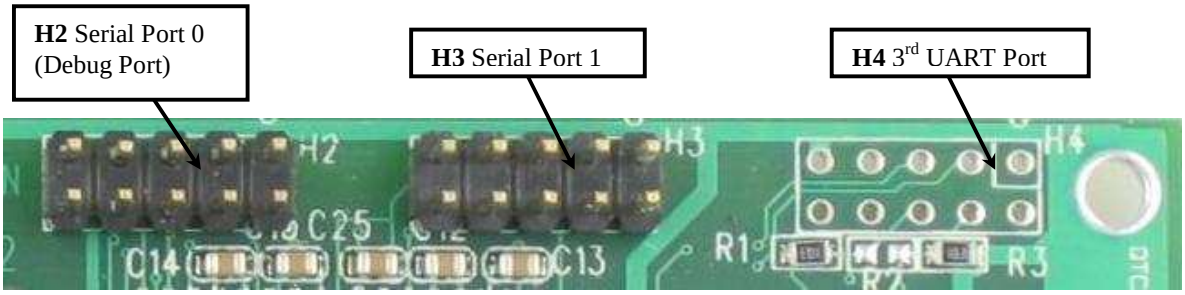
3.1 Engine controllers

The ***P52*** was designed to be driven by a Tern host controller, using the 16-bit external data/address bus to drive the parallel ADC and DAC, as well as other components. Any 'Engine' used will be installed on top of the ***P52*** via 20x2 pin headers J1 and J2, and can be secured by two #4-40 mounting screws.

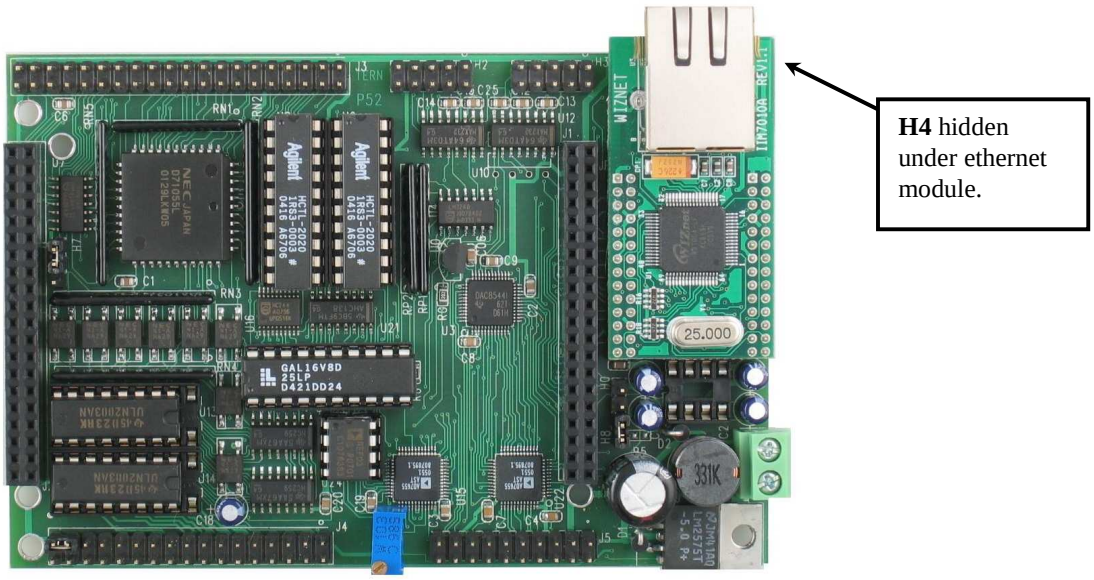
3.2 Serial Ports Drivers

The ***P52*** can provide up to 3 channels RS-232/485 drivers. By default, two RS-232 drivers are ready for the two asynchronous serial UARTs from the installed Engine controller via 20x2 pin header J1 and J2. One optional 3rd RS232 or RS485 driver can be installed to support the optional UART SCC2691 on the Engine controller.

The default debug serial port SER0 is routed at H2, SER1 at H3, and SCC port at H4.



Note: H4 is hidden beneath the Wiznet Ethernet Module. If the Ethernet is installed while H4 is needed, an angled header should be considered.



3.3 I/O Mapped Devices

3.3.1 I/O Space

External I/O devices can use I/O mapping for access. You can access such I/O devices with ***inportb(port)*** or ***outportb(port,dat)*.** These functions will transfer one byte of data to the specified I/O address. Refer to the software chapter of the controlling Engine's technical manual for additional information on I/O space and access.

The tables below shows more information about I/O mapping,

I/O space	Select Signal	Location	Usage
0x00,02,04,06	/PP1	U1 pin 7	/PPI for PPI
0x10 /RD	/AD	U15 pin 31	/AD for AD7655
0x20 /RD	/AD1	U22 pin 31	/AD1 for AD7655
0x10 /WR	LD	U3 pin 27	LD for DA8544
0x20 /WR	/DA	U3	/DA for DA8544
0x30 /WR	/ADR	U2 pin 11	/ADR for ethernet
0x40 /RD	/RDT	U16 pin 1	/RDT read optos
0x48 /RD	/HP1	U6 pin 4	read HP2020 (U6)
0x50	/HP2	U8 pin 4	read HP2020(U8)
0x60 /WR	/HV1	U23 pin 4	write HC259 (U23)
0x68	/HV2	U24 pin 4	write HC259 (U24)
0x70	/CV	U15 pin 35	/CV for AD7655 (U15)
0x78	/CV1	U22 pin 35	/CV1 for AD7655 (U22)

Table 3.1 186-Engine Mapping

I/O space	Select Signal	Location	Usage
0x1080,82,84,86	/PP1	U1 pin 7	/PPI for PPI
0x1090 /RD	/AD	U15 pin 31	/AD for AD7655
0x10A0 /RD	/AD1	U22 pin 31	/AD1 for AD7655
0x1090 /WR	LD	U3 pin 27	LD for DA8544
0x10A0 /WR	/DA	U3	/DA for DA8544
0x10B0 /WR	/ADR	U2 pin 11	/ADR for ethernet
0x10C0 /RD	/RDT	U16 pin 1	/RDT read optos
0x10C8 /RD	/HP1	U6 pin 4	read HP2020 (U6)
0x10D0	/HP2	U8 pin 4	read HP2020(U8)
0x10E0 /WR	/HV1	U23 pin 4	write HC259 (U23)
0x10E8	/HV2	U24 pin 4	write HC259 (U24)
0x10F0	/CV	U15 pin 35	/CV for AD7655 (U15)
0x10F8	/CV1	U22 pin 35	/CV1 for AD7655 (U22)

Table 3.2 586-Engine Mapping

3.3.2 Programmable Peripheral Interface (82C55A)

The U1 PPI (8255) is a low-power CMOS programmable parallel interface unit for use in microcomputer systems. It provides 24 I/O pins that may be individually programmed in two groups of 12 and used in three major modes of operation.

In MODE 0, the two groups of 12 pins can be programmed in sets of 4 and 8 pins to be inputs or outputs. In MODE 1, each of the two groups of 12 pins can be programmed to have 8 lines of input or output. Of the 4 remaining pins, 3 are used for handshaking and interrupt control signals. Finally, MODE 2 is a strobed bi-directional bus configuration.

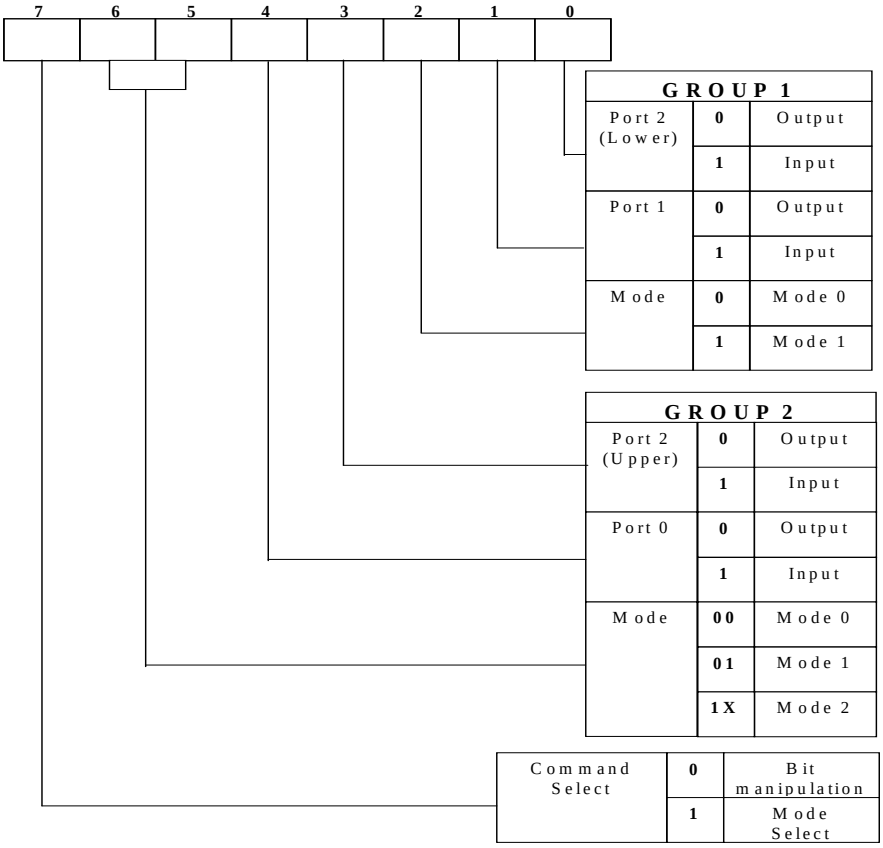


Figure 3.1 Mode Select Command Word

P52 maps U1, the PPI 8255, at base I/O address PPI = 0x1080 (586-Engine) and 0x00 (186-Engine).

All ports/registers are offsets of this I/O base address.

The Command Register address = PPI+6; Port 0 address = PPI+0; Port 1 address = PPI+2;

and Port 2 address = PPI+4.

The following code example will set all ports to output mode:

```
outportb(PPI+6,0x80);  /* Mode 0 all output selection. */
```

And then write to specific pins after setup:

```
outportb(PPI+0,0x55);  /* Sets port 0 to alternating high/low I/O pins. */
outportb(PPI+2,0x55);  /* Sets port 1 to alternating high/low I/O pins. */
outportb(PPI+4,0x55);  /* Sets port 2 to alternating high/low I/O pins. */
```

To set all ports to input mode:

```
outportb(PPI1+6,0x9f);     /* Mode 0 all input selection. */
```

You can read the ports with:

```
inportb(PPI+0); /* Port 0 */
inportb(PPI+2); /* Port 1 */
inportb(PPI+4); /* Port 2 */
```

These *inport(PPI+i);* statements return an 8-bit value for each port, with each bit corresponding to the appropriate line on the port.

There are 24 TTL level I/O pins free to use for your application. These I/O lines are specified as 4 mA driving current capability. PPI outputs are routed to J3.1-24. See schematics for PPI connection header J3 .

3.3.3 HCTL2020

Two quadrature decoder/counter interface chips, (HCTL2020, Hewlett Packard, U6 and U8) can be installed on the ***P52***. The quadrature decoder is used to interface incremental motion encoders with the microprocessor system or to improve system performance for digital closed-loop motion control systems. The HCTL2020 includes a quadrature decoder, a 16-bit counter, and an 8-bit bus interface. It features full 4x decoding, up to 14 MHz clock operation, high noise immunity due to Schmitt-trigger inputs and digital noise filters, quadrature decoder output signals, up/down signal, count signals, and cascade output signal. Many types of optical incremental encoder modules, such as the HEDS-9000, HEDS-9100, and HEDS-9200 from HP, can be directly interfaced to the HCTL2020.

Channel A and B signals buffered with Schmitt trigger inputs (U7, 74HC14, CHA1/2, CHB1/2) are routed at pins 31, 32, 35, and 36 on header J3. The HCTL2020 has built-in filters, which allow reliable operation in noisy environments.

3.3.4 Four channel, 16-bit ADC (AD7655)

Two AD7655 ADC's may be installed on the ***P52.*** The unique 16-bit parallel ADC (AD7655, 0-5V) supports ultra high-speed (1 MHz conversion rate) analog signal acquisition. The AD7655 contains two low noise, high bandwidth track-and-hold amplifiers that allow *simultaneous* sampling on two channels. Each track-and hold amplifier has a multiplexer in front to provide a total of 4 channels analog inputs. The parallel ADC achieves very high throughput by requiring only two CPU I/O operations (one start, one read) to complete a 16-bit ADC reading. With a precision external 2.5V reference, the ADC accepts 0-5V analog inputs at 16-bit resolution of 0-65,535. U22 inputs are found on J5.7-10, while U15 inputs are on J5.11-14.

See sample program "*p52_ad.c*" in **\tern\186\samples\p52** or **\tern\586\samples\p52** for details on reading the ADC. The sample program is also included in the pre-built sample project "*p52.ide*" in **\tern\186\samples\p52** and **\tern\586\samples\p52**.

Refer to the data sheet for additional specifications; \tern_docs\parts\ad7655.pdf.

3.3.5 Four channel, 16-bit DAC (DA8544)

The DA8544 is a parallel 16-bit D/A converter. This device supports 4 voltage output channels buffered by ops with hardware configurable gain (default gain=2), giving default output range of ±5V. An on-board pot allows for adjustable analog output voltage. The DAC requires an external 5V reference given by a precision reference installed at U0.

The ***P52*** uses data bus D15 to D0 to directly interface to the DAC's full 16-bit data bus for maximum data transfer rate. Four outputs are routed to J5.17-20.

A sample program "*p52_da.c*" is in the **\tern\186\samples\p52** and **\tern\586\samples\p52** directory.

3.3.6 100 MHz Base-T Ethernet

An WizNet™ Fast Ethernet Module can be installed to provide 100M Base-T network connectivity. This Ethernet module has a hardware LSI TCP/IP stack. It implements TCP/IP, UDP, ICMP and ARP in hardware, supporting internet protocol DLC and MAC. It has 16KB internal transmit and receiving buffer which is mapped into host processor's direct memory. The host can access the buffer via high speed DMA transfers. The hardware Ethernet module releases internet connectivity and protocol processing from the host processor. It supports 4 independent stack connections simultaneously at a 4Mbps protocol processing
speed. An RJ45 8-pin connector is on-board for connecting to 10/100 Base-T Ethernet network. A software
library is available for Ethernet connectivity.

3.3.7 Opto-couplers

There are 8 opto-couplers on the ***P52***. These opto-couplers provide optical isolation and can be used for digital inputs, relay contact monitor, or powerline monitor. These optos have a 3 micro-second ON time and 5 micro-second OFF time. The on-board input pins have a 1kΩ pullup, so a low input signal will turn the coupler ON. Opto-coupler intputs are routed to pins J4.1-8.

3.3.8 High-Voltage, High-Current Drivers

ULN2003 (U13 and U14) are high voltage, high current Darlington transistor arrays, consisting of 7 silicon NPN Darlington pairs on a common monolithic substrate. All channels feature open-collector outputs for sinking 350 mA at 50V, and integral protection diodes for driving inductive loads. Peak inrush currents of up to 600 mA sinking are allowed. Outputs may be paralleled to achieve high-load capability, although each driver has a maximum continuous collector current rating of 350 mA at 50V. The maximum power dissipation allowed is 2.20 W per chip at 25 degrees C. The common substrate VS is routed to J4 pin 31. All currents sinking in must return to the J4 pin 31, which should be shorted to GND. A heavy gage(20) wire must be used to connect the GND terminal to an external common ground return. K connects to the protection diodes in the ULN2003 chips and should be tied to highest voltage in the external load system. K can be connected to an unregulated on board +12V. **ULN2003 is a sinking driver not sourcing driver.** Typical application wiring is shown below.

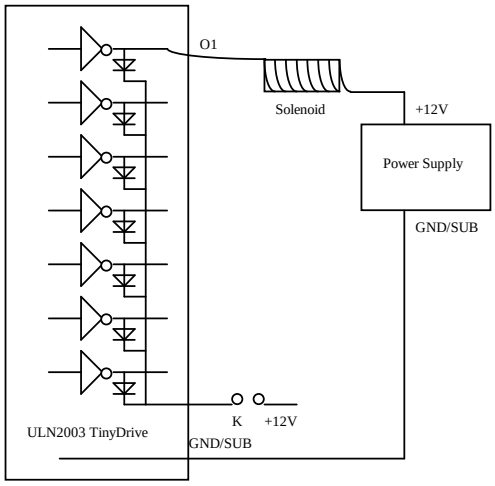


Figure 3.2 Drive inductive load with high voltage/current drivers.

3.4 Headers and Connectors

Two 20x2, 0.1 spacing sockets are installed on the ***P52***.

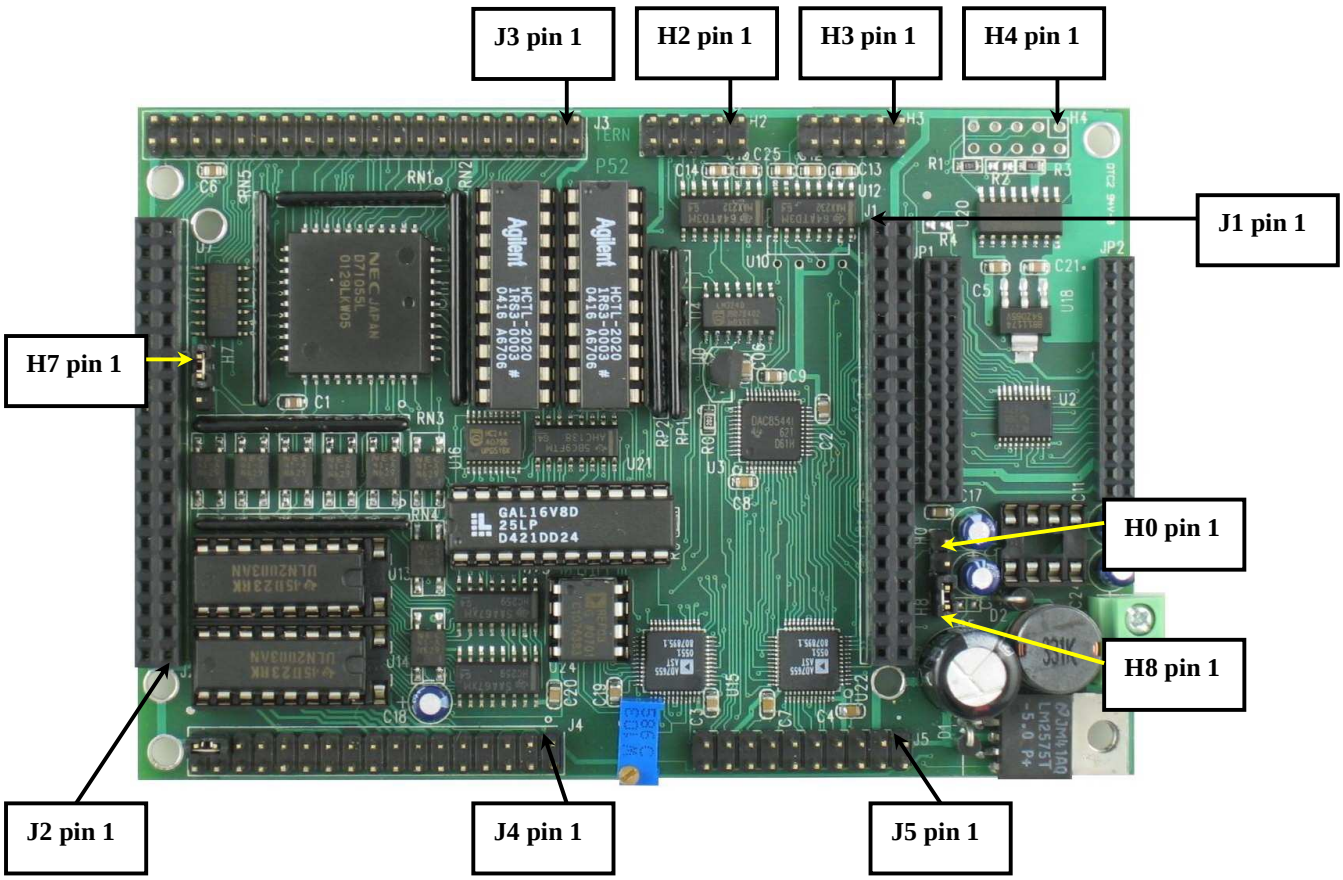


Figure 3.3 Pin header locations

3.4.1 Jumpers and Headers

The jumpers and connectors on the P50 are listed below.

Name	Size	Function	Possible Configuration
J1	20x2	main expansion port	
J2	20x2	main expansion port	
J3	20x2	PPI TTL I/Os / Q.D. signals	PPI(U1), Q.D.(U6 and U8)
J4	17x2	HV and opto-couplers	HV(U13 and U14), opto (P1-P8)
J5	10x2	ADC and DAC lines	ADC(U15), ADC(U22) , DAC(U3)
H0	2x1	+12V	Jumpers V+ from U19 to +12V. Board **should not** take in any voltage higher than 12 Volts!
H1	2x1	+VI, GND	Input voltage to board
H2	5x2	SER0 (DEBUG), RS232	
H3	5x2	SER1, RS232	
H4	5x2	SCC2691: RS232/485 TXD, RXD, GND	Install RS232 or RS485 driver for 3rd UART on the host controller
H7	3x1	Ethernet chip select selector	586-Engine, jumper on pins 1&2
H8	2x1	VOFF	Jumpers VOFF to Ground

3.4.2 Expansion Headers J1 and J2

J2 Signal			
GND	40	39	VCC
	38	37	/ET
	36	35	
TXD0	34	33	/INT
RXD0	32	31	/RTS1
	30	29	
TXD1	28	27	
RXD1	26	25	
	24	23	P22
/CTS1	22	21	P21
	20	19	
	18	17	
	16	15	
	14	13	
	12	11	
	10	9	
	8	7	
	6	5	
	4	3	
GND	2	1	

J1 Signal			
VCC	1	2	GND
MPO	3	4	CLK
RXD	5	6	GND
TXD	7	8	D0
VOFF	9	10	D1
	11	12	D2
D15	13	14	D3
/RST	15	16	D4
RST	17	18	D5
/CS6	19	20	D6
D14	21	22	D7
D13	23	24	GND
	25	26	A7
D12	27	28	A6
/WR	29	30	A5
/RD	31	32	A4
D11	33	34	A3
D10	35	36	A2
D9	37	38	A1
D8	39	40	A0

Table 3.1 J1 and J2, 20x2 expansion ports for P52

Signal definitions for J1:

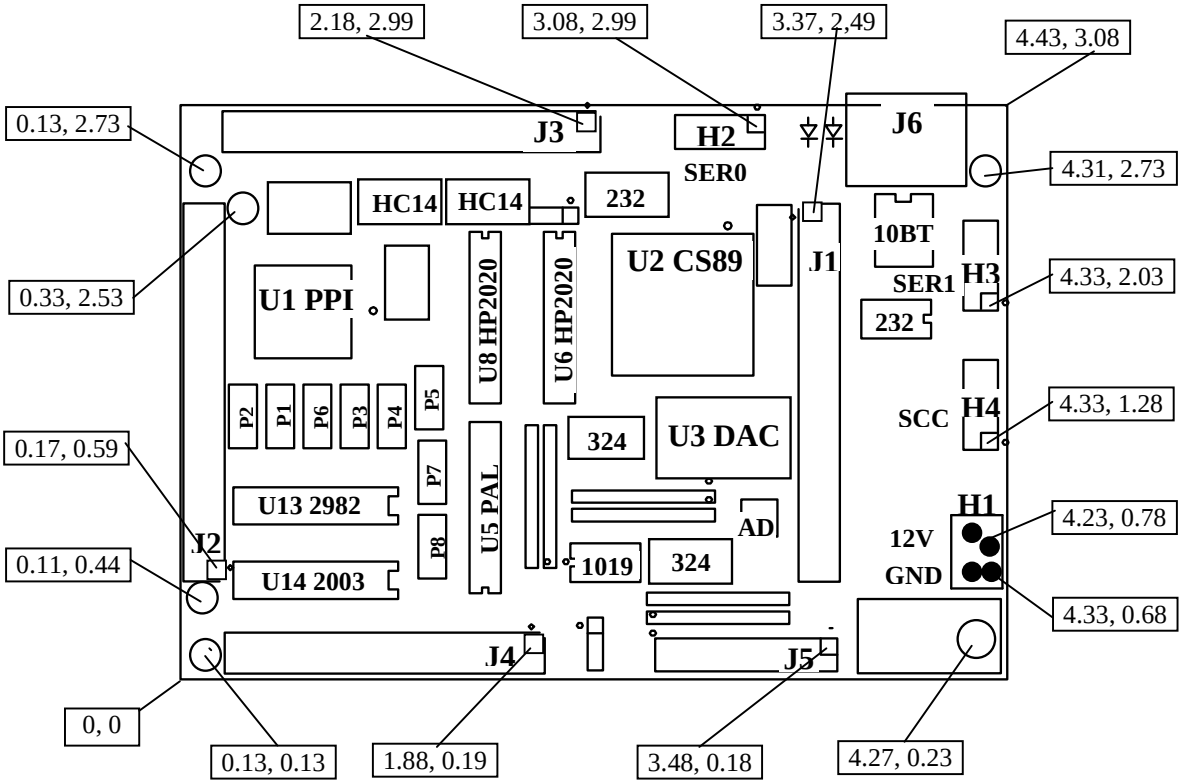
VCC	+5V power supply
GND	Ground
CLK	Software programmable clock output from host

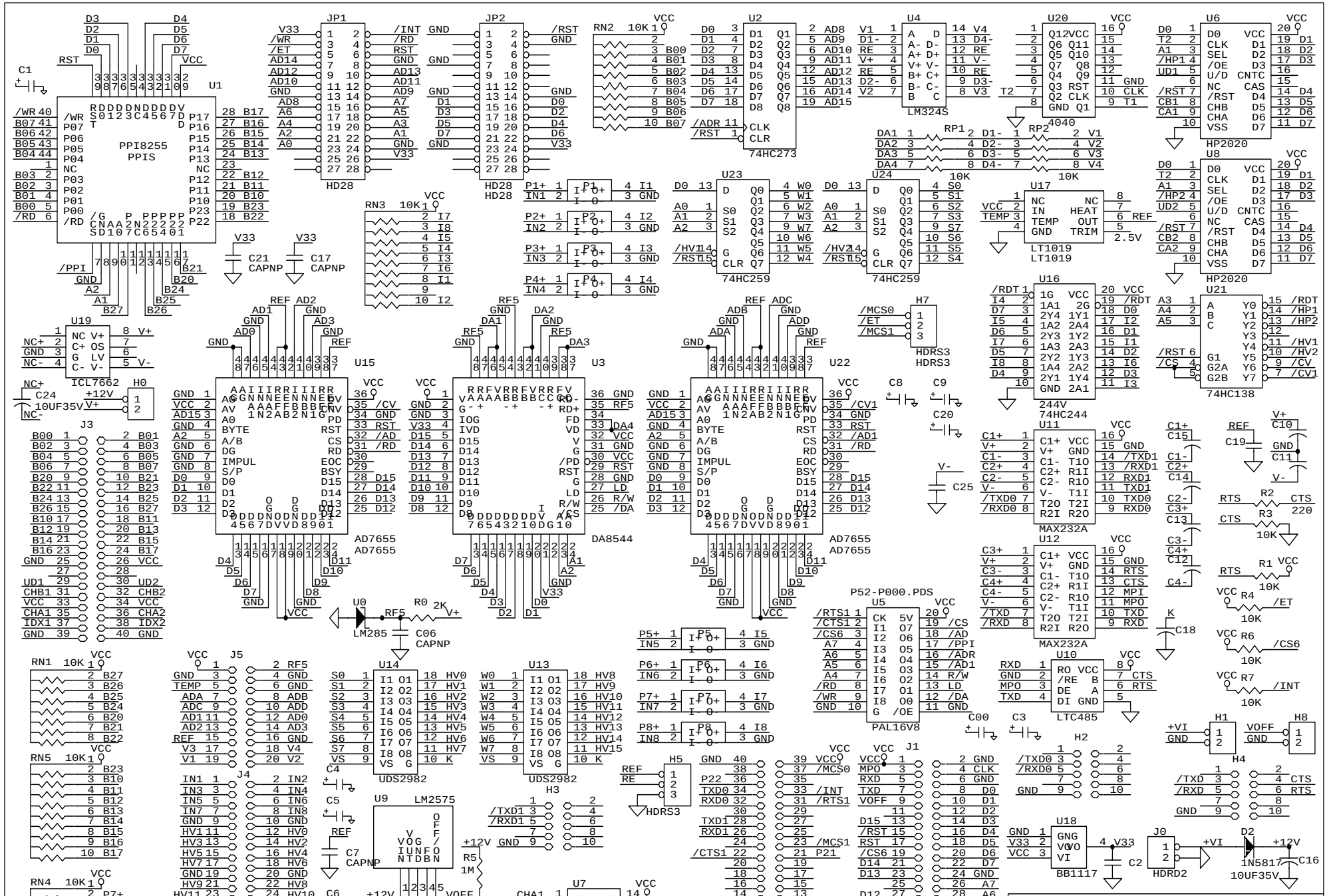
RxD	data receive of UART SCC2691
TxD	data transmit of UART SCC2691
MPO	Multi-Purpose Output of SCC2691
VOFF	real-time clock output
D0-D15	external data bus
A7-A0	lower address lines
/RST	reset signal, active low
RST	reset signal, active high
/CS6	8-bit chip select on the host
/WR	active low when write operation
/RD	active low when read operation

Signal definitions for J2:

VCC	+5V power supply
GND	Ground
Pxx	PIO pins
TxD0	transmit data of serial channel 0
RxD0	receive data of serial channel 0
TxD1	transmit data of serial channel 1
RxD1	receive data of serial channel 1
/CTS1	Clear-to-Send signal for SER1
/RTS0	Request-to-Send signal for SER0
/RTS1	Request-to-Send signal for SER1

Appendix A: P52 mechanical dimensions




U1 PPI8255 PPIS
JP1 HD28
JP2 HD28
U2 74HC273
U4 LM324S
U20 4040
U6 HP2020
U8 HP2020
U23 74HC259
U24 74HC259
U17 LT1019
U16 244V 74HC244
U21 74HC138
U19 ICL7662
U15 AD7655
U3 DA8544
U22 AD7655
U11 MAX232A
U12 MAX232A
U5 PAL16V8
U10 LTC485
U14 UDS2982
U13 UDS2982
U9 LM2575
U7 74HC14
U18 BB1117
J3
J5
J4
J1
J2
H3
H4
H5
H7
H8
H0
H1
H2
J0
D1 1N5817
D2 1N5817
LM285
ULN2003 VS=GND K=+VI
UDS2982 VS=+VI K=GND
TERN/STE
Title
ET, I/O, DAC, ADC, HV, OPTO
Size B
Document Number P52.SCH
REV
Date: February 19, 2007
Sheet 1 of 1